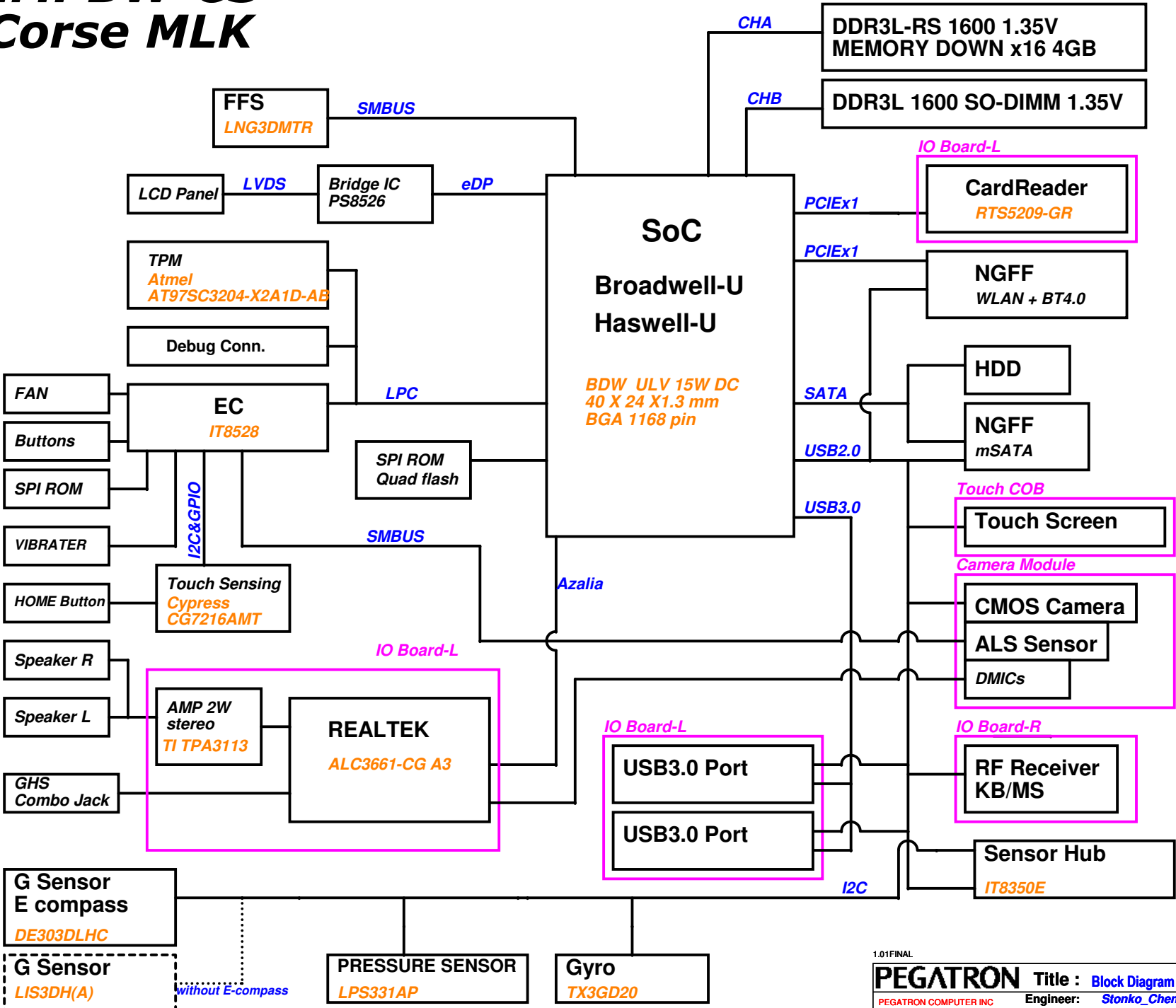


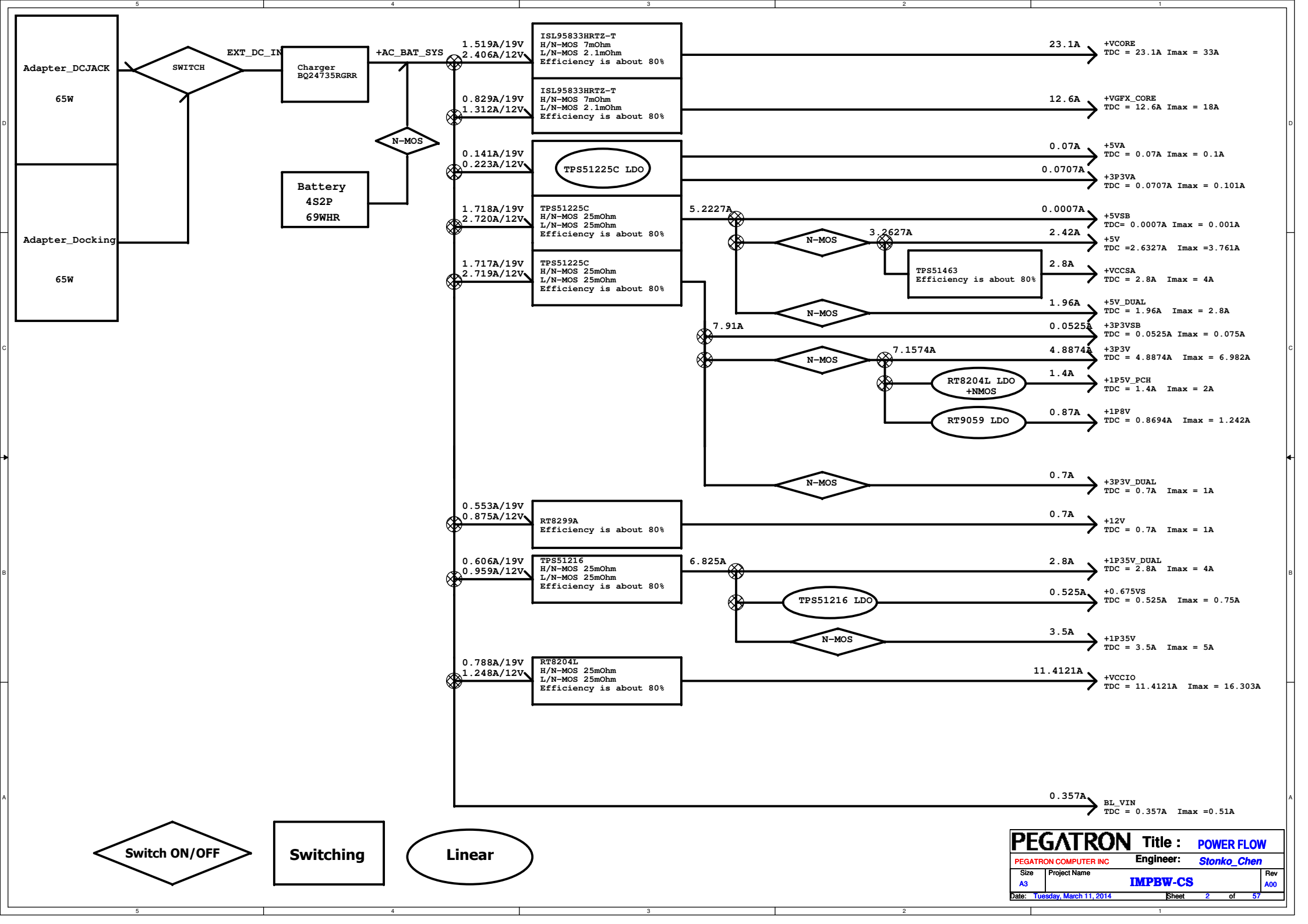
SYSTEM PAGE REF.

- 01. Block Diagram
- 02. POWER FLOW
- 03. Power On Sequence
- 04. Power On Timing
- 05. CPU(1)_MISC.JTAG,DDI.EDP
- 06. CPU(2)_DDR3L-RS
- 07. CPU(3)_HSW POWER
- 08. CPU(4)_GND
- 09. CPU(5)_RESERVED
- 10. CPU(6)_XDP
- 11. DDR3L-RS_Memory Down
- 12. DDR3L-RS_SO-DIMM
- 13. DDR3L-RS_Decoupling
- 14. DDR3L-RS_CA/DQ Voltage
- 15. PCH_SATA, IHDA, RTC
- 16. PCH_CLK, SMB, LPC
- 17. PCH_FDI, DMI, SYS_PWR
- 18. PCH_DP, PCI
- 19. PCH_PCIE, NVRAM, USB
- 20. PCH_CPU, GPIO, MISC
- 21. PCH_POWER, GND
- 22. PCH_SPI, SMB
- 23. shippingmode
- 24. NGFF_CARD_WLAN
- 25. NGFF_CARD_mSATA
- 26. SATA redriver
- 27. SATA conn
- 28. eDP_ANX1122
- 29. LVDS
- 30. USB3.0 redriver
- 31. USB Touch
- 32. ALS, CAMERA, DMIC
- 33. RIO LIO connector
- 34. Homekey_connector
- 35. Sensor_Hub_IT8350E
- 36. Gyro&G&Pressure-sensor
- 37. FFS
- 38. ITE 8528-1
- 39. ITE 8528-2
- 40. TPM
- 41. VIBRATER
- 42. THERMAL / FAN
- 43. RST_Reset Circuit
- 44. BUG_Debug
- 45. DSG_Discharge
- 46. SCREW HOLE
- 47. POWER_PROTECT
- 48. DC_DC/BAT CONN
- 49. DC IN
- 50. +AC_BAT_SYS & Charger
- 51. +VCORE
- 52. +VCORE1
- 53. +3P3VSB/+5VSB
- 54. +1P35V_DUAL/+VTT_DDR
- 55. +1P05V
- 56. +1P5V
- 57. Switch

IMPBW-CS
Corse MLK

Block Diagram





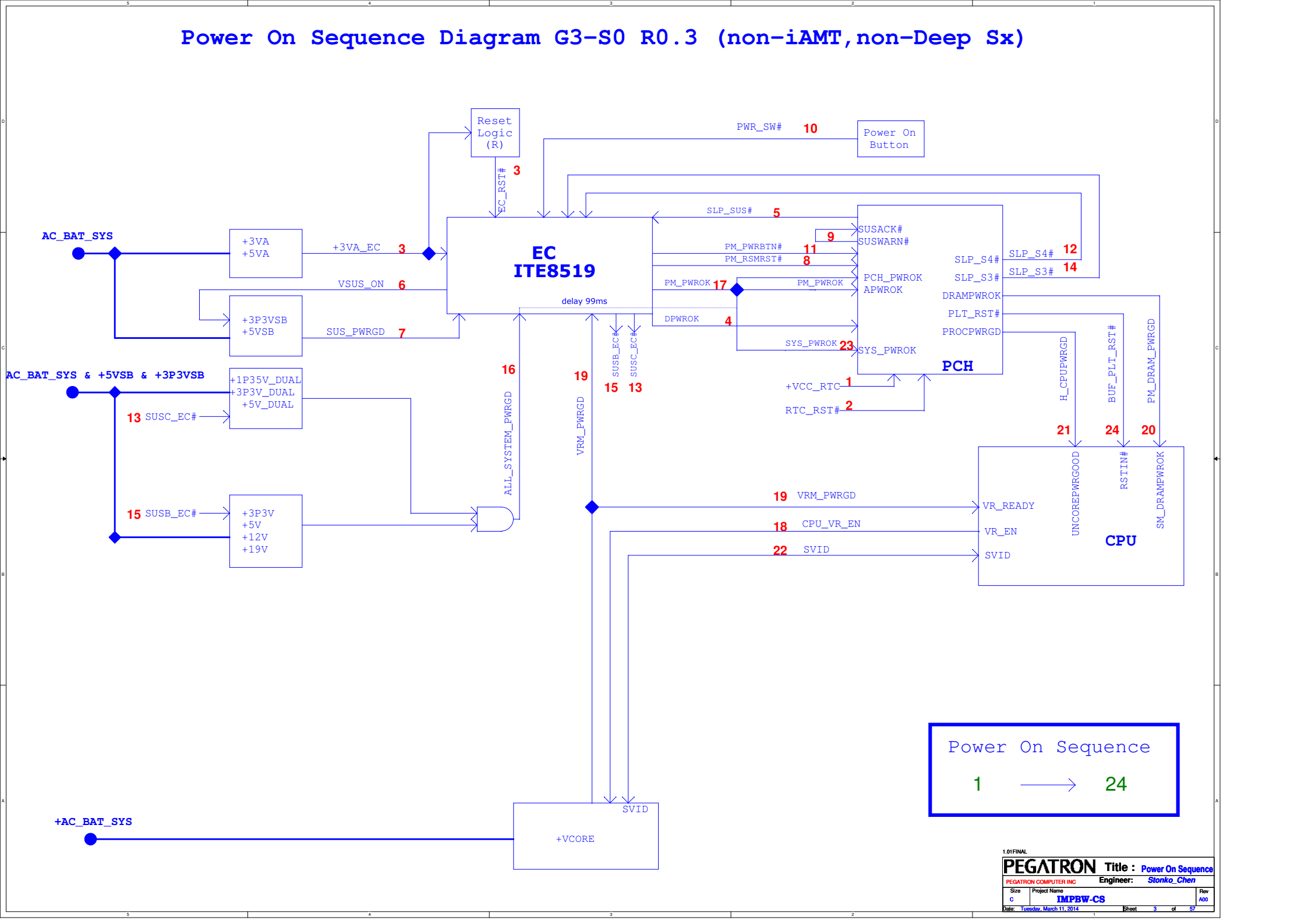
The diagram illustrates the power-on sequence for a system with an EC ITE8519, PCH, and CPU. The sequence starts with the AC_BAT_SYS signal, which triggers the +3VA and +5VA regulators. The +3VA regulator outputs +3VA_EC (pin 3) to the EC. The +5VA regulator outputs VSUS_ON (pin 6) to the EC. The +3P3VSB and +5VSB regulators output SUS_PWRGD (pin 7) to the EC. The EC also receives a Reset Logic (R) signal (pin 3) and a PWR_SW# signal (pin 10) from the Power On Button. The EC outputs SLP_SUS# (pin 5) to the PCH. The PCH outputs SUSACK# (pin 9) and SUSWARN# (pin 11) to the EC. The PCH also outputs PM_PWRBTN# (pin 11) and PM_RSMRST# (pin 8) to the EC. The PCH outputs PM_PWROK (pin 17) and DPWROK (pin 4) to the EC. The PCH outputs SYS_PWROK (pin 23) to the EC. The PCH outputs SLP_S4# (pin 12) and SLP_S3# (pin 14) to the CPU. The PCH outputs DRAMPWROK, PLT_RST#, and PROCPWROK to the CPU. The CPU outputs H_CPUPWROK (pin 21) to the PCH. The CPU outputs BUF_PLT_RST# (pin 24) to the PCH. The CPU outputs PM_DRAMPWROK (pin 20) to the PCH. The CPU outputs VR_READY (pin 19), VR_EN (pin 18), and SVID (pin 22) to the VRM_PWRGD signal. The VRM_PWRGD signal is also connected to the EC. The EC outputs ALL_SYSTEM_PWRGD (pin 16) to the VRM_PWRGD signal. The VRM_PWRGD signal is connected to the +VCORE regulator. The +VCORE regulator outputs +VCORE to the CPU. The CPU outputs SVID (pin 22) to the +VCORE regulator. The sequence ends with the CPU outputting SVID (pin 22) to the +VCORE regulator.

Power On Sequence

1 → 24

1.01 FINAL

PEGATRON		Title : Power On Sequence	
PEGATRON COMPUTER INC		Engineer: Stonko_Chen	
Size	Project Name	Rev	
C	IMPBW-CS	A00	
Date: Tuesday, March 11, 2014	Sheet	3	of 57



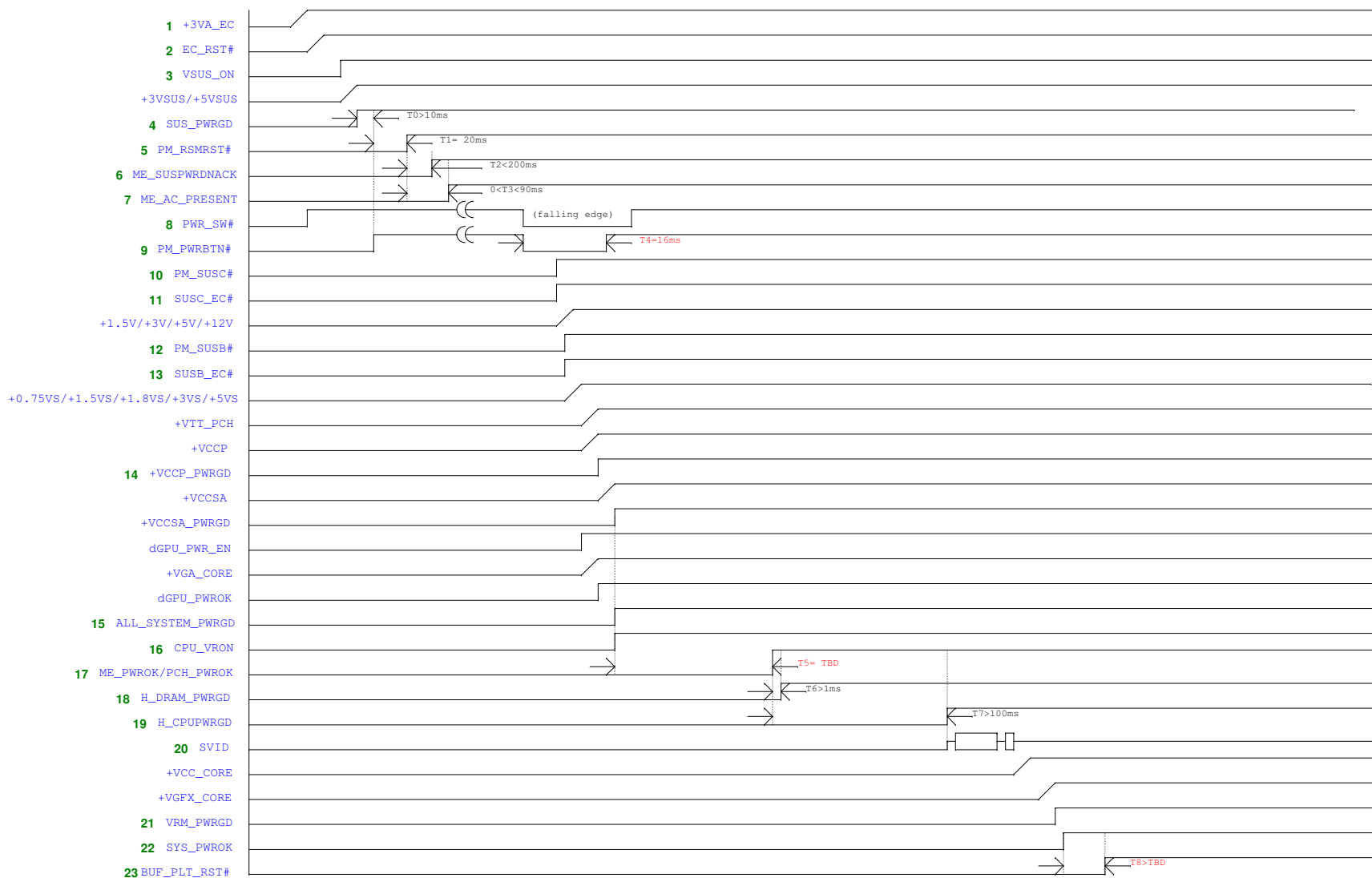
Power On Sequence

1 → 24

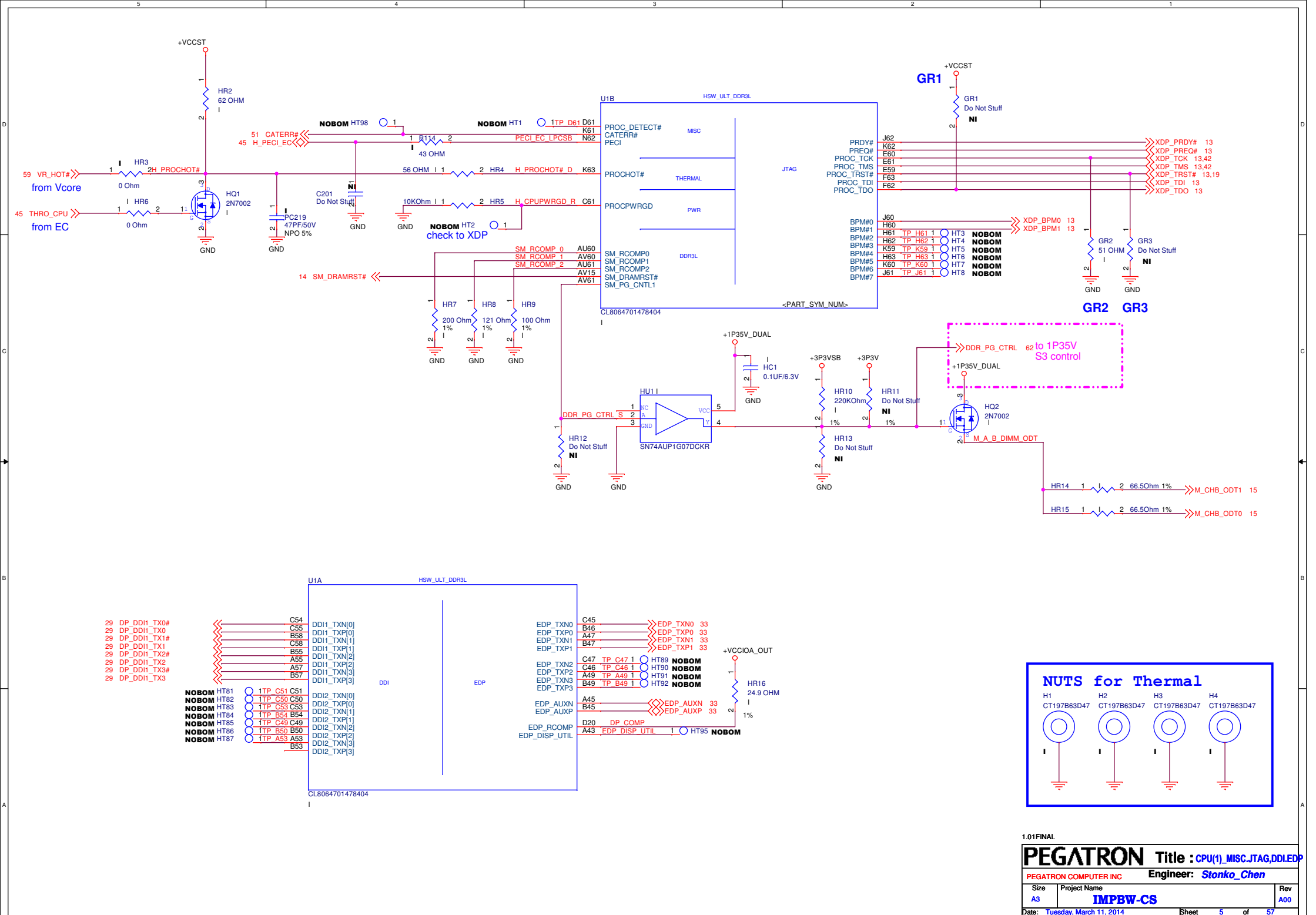
Power On Sequence

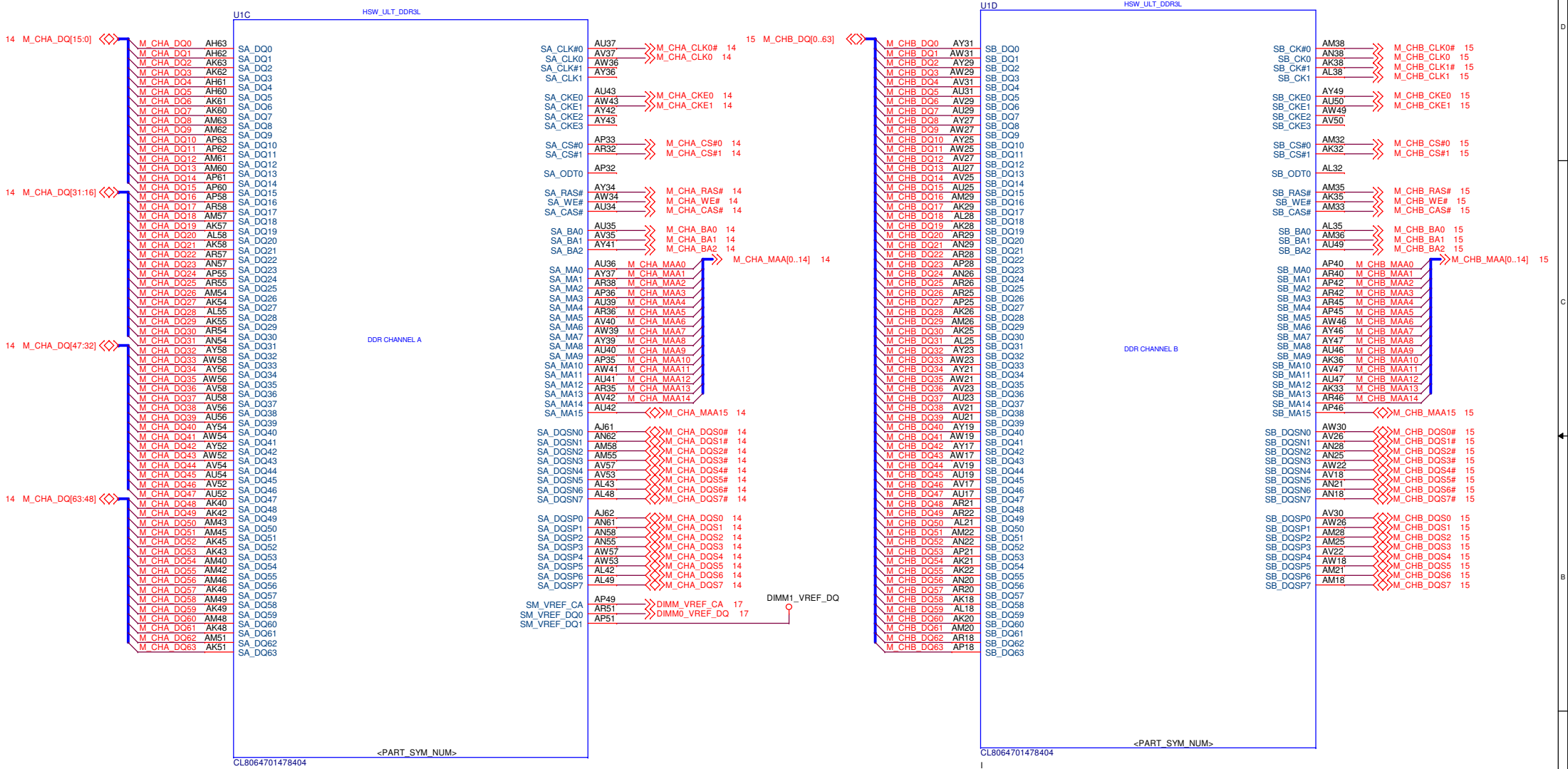
1 → 24

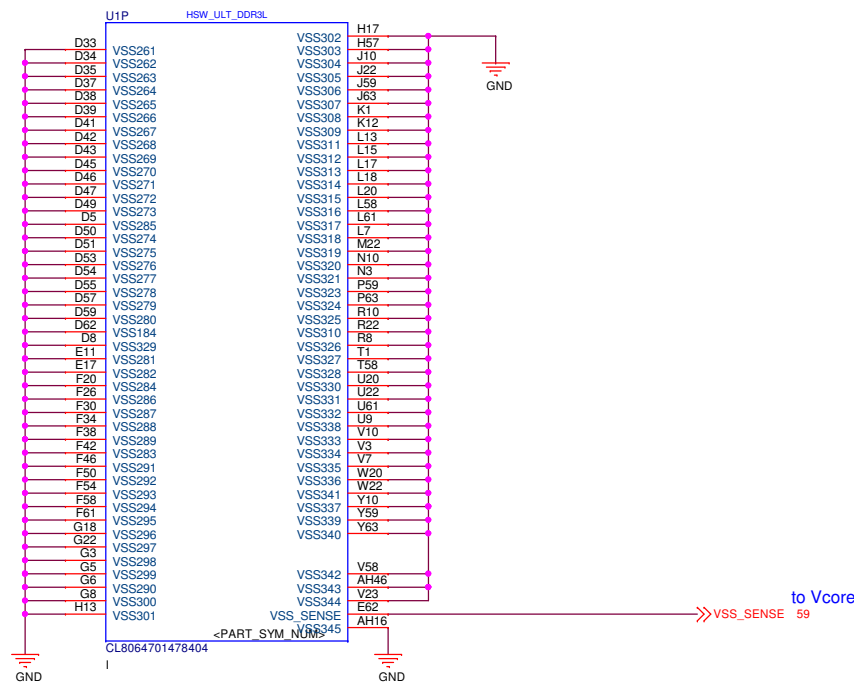
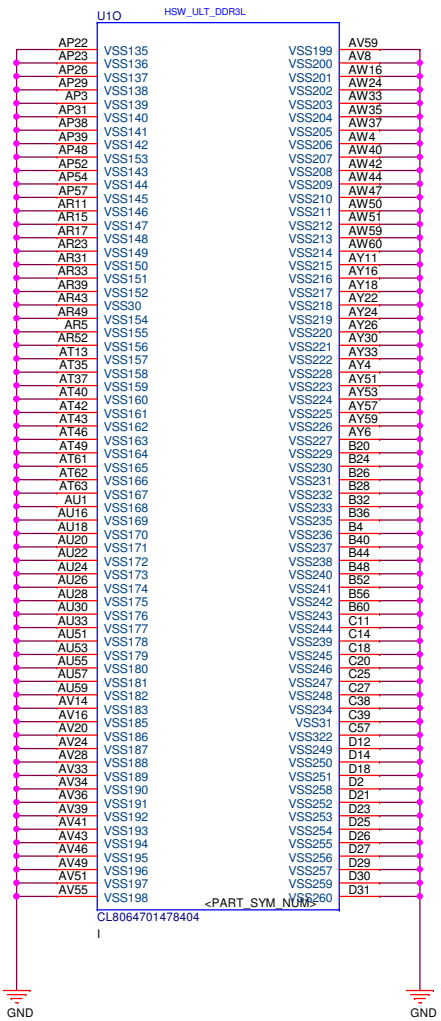
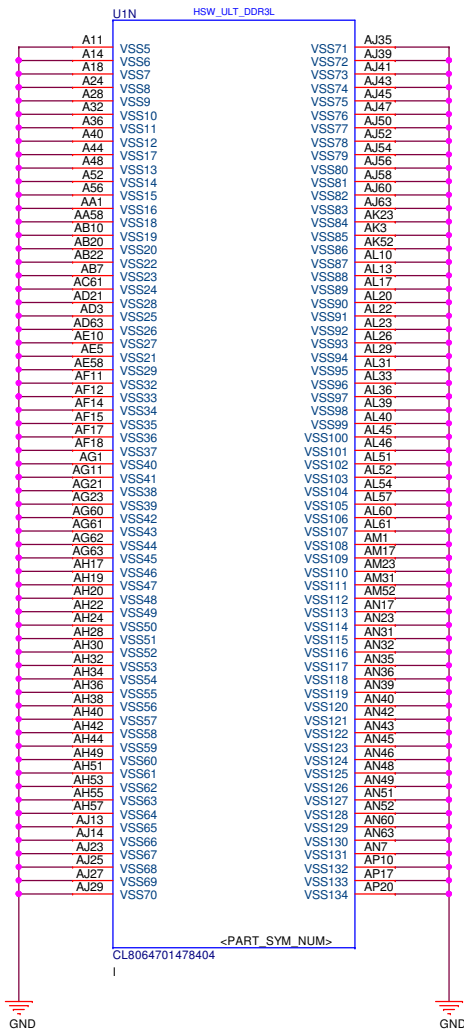
Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



1.01 FINAL







CFG strapping information:

The CFG signals have a default value of '1'
CFG[20:0] - INT. PU

CFG[3:0]: Reserved configuration lane.

A test point may be placed on the board for these lanes.

CFG[4]: eDP enable

-1 = Disabled
-0 = Enabled

CFG[19:5]: Reserved configuration lanes.

A test point may be placed on the board for these lands.

Follow Harris Beach

CFG strapping information:

The CFG signals have a default value of '1'

CFG[0]: EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED

-1 = (DEFAULT) NORMAL OPERATION; NO STALL
-0 = STALL

CFG[1]: PCH/ PCH LESS MODE SELECTION

-1 = (DEFAULT) NORMAL OPERATION
-0 = PCH-LESS MODE

CFG[8]: ALLOW THE USE OF NOA ON LOCKED UNITS

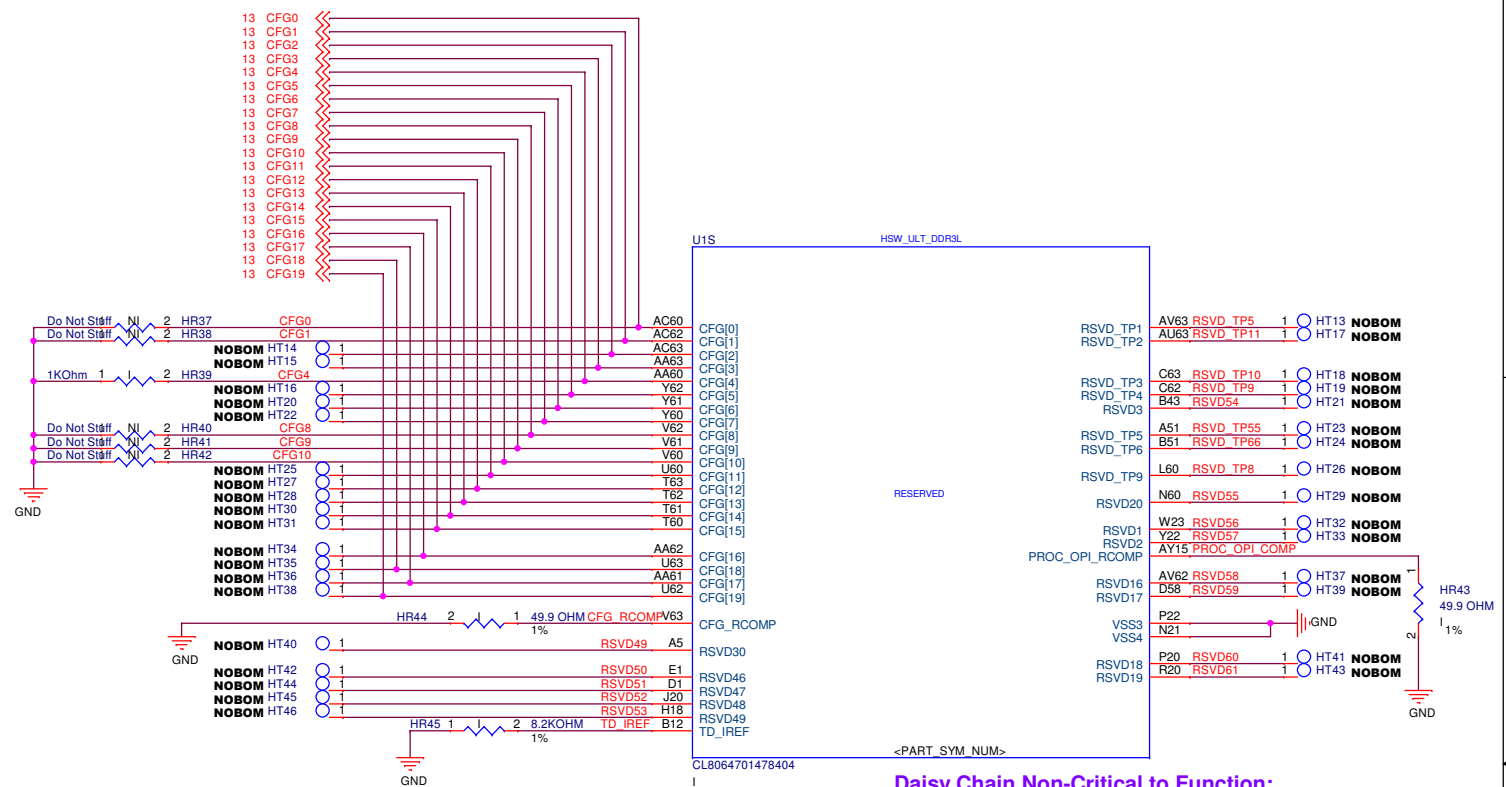
-1 = DISABLED(DEFAULT);
IN THIS CASE, NOA WILL BEDISABLED IN LOCKED UNITS
AND ENABLED IN UN-LOCKED UNITS
-0 = ENABLED;
NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT

CFG[9]: NO SVID PROTOCOL CAPABLE VR CONNECTED

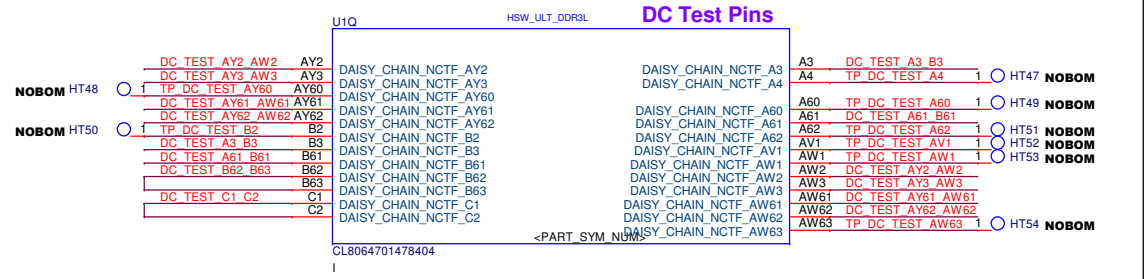
-1 = VRS SUPPORTING SVID PROTOCOL ARE PRESENT
-0 = NO VR SUPPORTING SVID IS PRESENT.
THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY

CFG[10]: SAFE MODE BOOT

-1 = POWER FEATURES ACTIVATED DURING RESET
-0 = POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

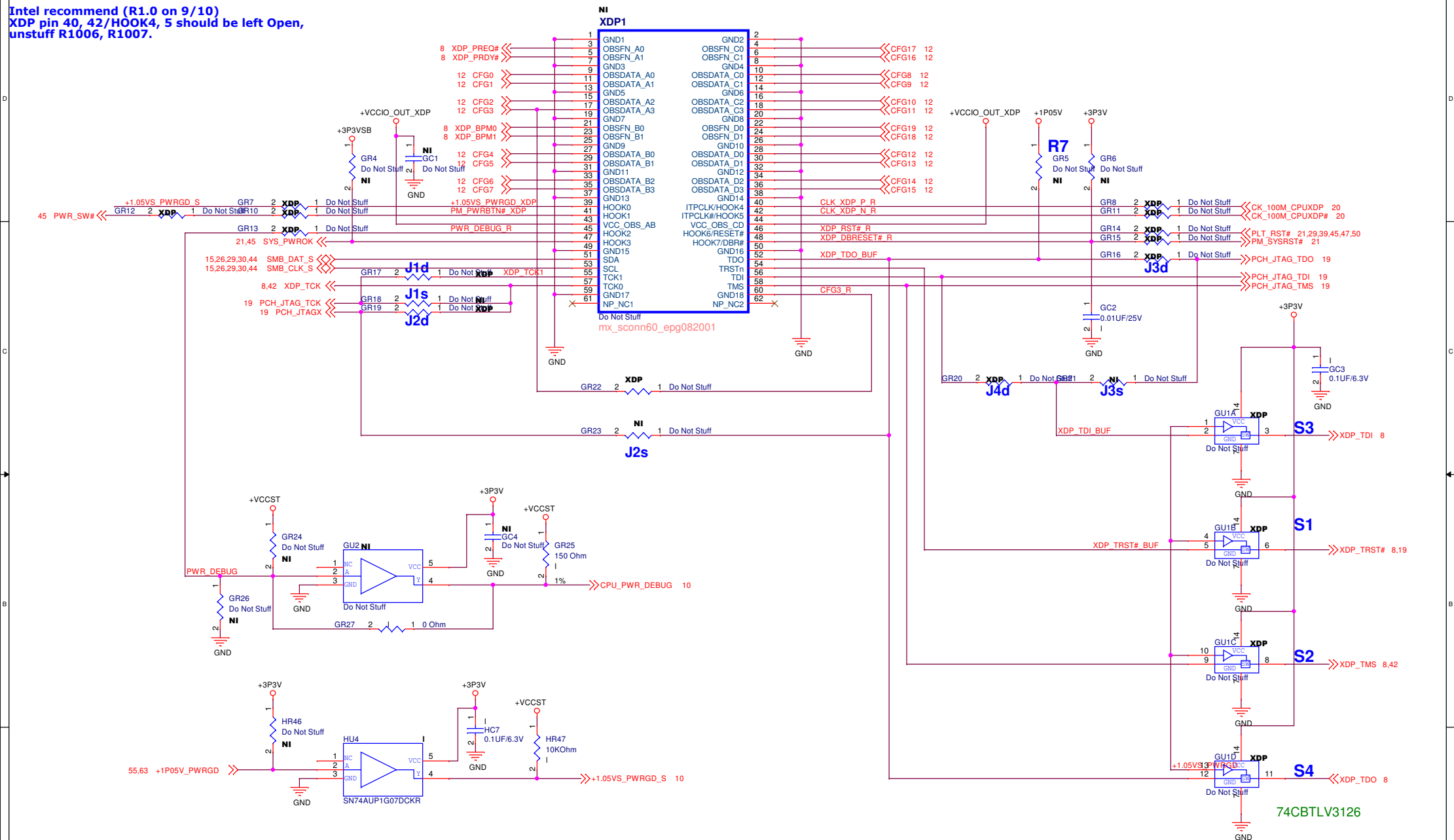


Daisy Chain Non-Critical to Function:
These signals are for BGA solder joint reliability testing and are non-critical to function.



CPU XDP connector

**Intel recommend (R1.0 on 9/10)
XDP pin 40, 42/HOOK4, 5 should be left Open,
unstuff R1006, R1007.**



1.01FINAL

PEGATRON Title : CPU(6)_XDP

PEGATRON COMPUTER INC Engineer: Stonko_Chen

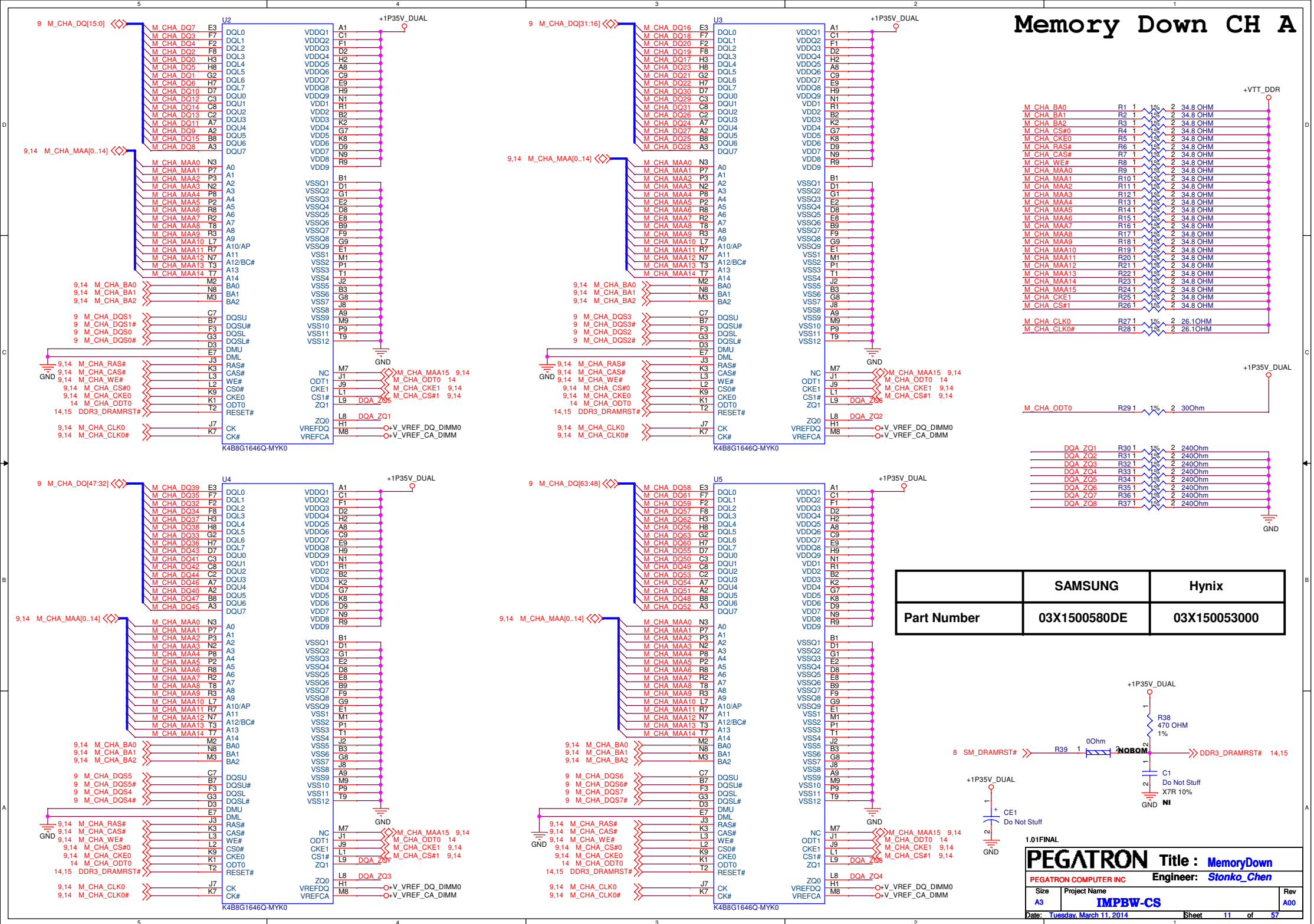
Size	Project Name	Rev
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A3 IMPBW-CS A00

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	1
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Memory	Down	CH	A
0000	0000	0000	0000
0001	0000	0000	0000
0002	0000	0000	0000
0003	0000	0000	0000
0004	0000	0000	0000
0005	0000	0000	0000
0006	0000	0000	0000
0007	0000	0000	0000
0008	0000	0000	0000
0009	0000	0000	0000
000A	0000	0000	0000
000B	0000	0000	0000
000C	0000	0000	0000
000D	0000	0000	0000
000E	0000	0000	0000
000F	0000	0000	0000
0010	0000	0000	0000
0011	0000	0000	0000
0012	0000	0000	0000
0013	0000	0000	0000
0014	0000	0000	0000
0015	0000	0000	0000
0016	0000	0000	0000
0017	0000	0000	0000
0018	0000	0000	0000
0019	0000	0000	0000
001A	0000	0000	0000
001B	0000	0000	0000
001C	0000	0000	0000
001D	0000	0000	0000
001E	0000	0000	0000
001F	0000	0000	0000
0020	0000	0000	0000
0021	0000	0000	0000
0022	0000	0000	0000
0023	0000	0000	0000
0024	0000	0000	0000
0025	0000	0000	0000
0026	0000	0000	0000
0027	0000	0000	0000
0028	0000	0000	0000
0029	0000	0000	0000
002A	0000	0000	0000
002B	0000	0000	0000
002C	0000	0000	0000
002D	0000	0000	0000
002E	0000	0000	0000
002F	0000	0000	0000
0030	0000	0000	0000
0031	0000	0000	0000
0032	0000	0000	0000
0033	0000	0000	0000
0034	0000	0000	0000
0035	0000	0000	0000
0036	0000	0000	0000
0037	0000	0000	0000
0038	0000	0000	0000
0039	0000	0000	0000
003A	0000	0000	0000
003B	0000	0000	0000
003C	0000	0000	0000
003D	0000	0000	0000
003E	0000	0000	0000
003F	0000	0000	0000
0040	0000	0000	0000
0041	0000	0000	0000
0042	0000	0000	0000
0043	0000	0000	0000
0044	0000	0000	0000
0045	0000	0000	0000
0046	0000	0000	0000
0047	0000	0000	0000
0048	0000	0000	0000
0049	0000	0000	0000
004A	0000	0000	0000
004B	0000	0000	0000
004C	0000	0000	0000
004D	0000	0000	0000
004E	0000	0000	0000
004F	0000	0000	0000
0050	0000	0000	0000
0051	0000	0000	0000
0052	0000	0000	0000
0053	0000	0000	0000
0054	0000	0000	0000
0055	0000	0000	0000



Memory SO-Dimm CH B

12X021893000

9 M_CHB_MAA[0..15] >>> M_CHB_DQ[0..63] 9

0~7 8~15 16~23 24~31 32~39 40~47 48~55 56~63

13.26.29.30.44 SMB_CLK_S
13.26.29.30.44 SMB_DAT_S

DDR3_DIMM_204P

H:4.0mm

place the cap near to dimm reset pin

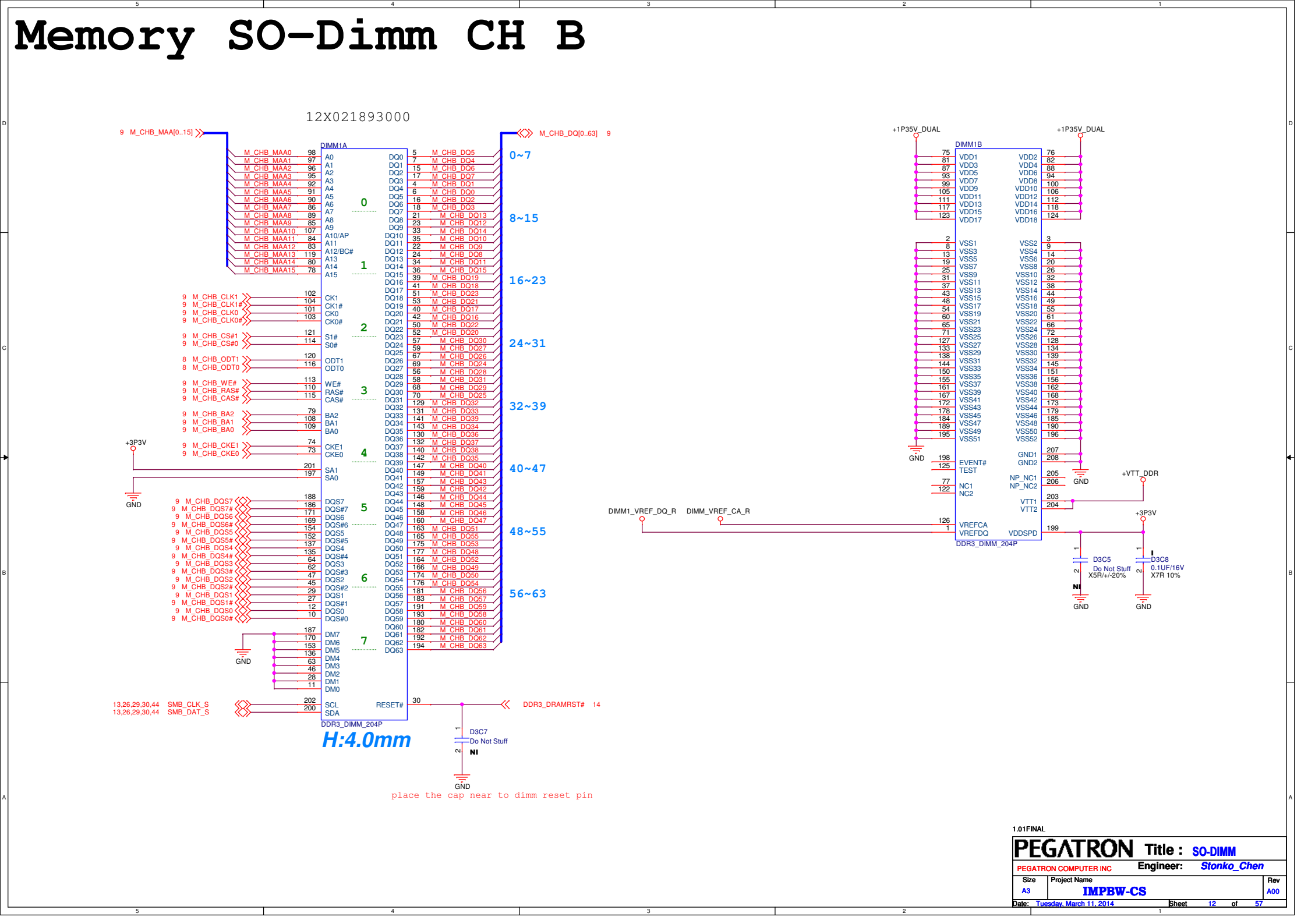
1.01FINAL

PEGATRON Title : SO-DIMM

PEGATRON COMPUTER INC Engineer: Stonko_Chen

Size A3 Project Name IMPBW-CS

Date: Tuesday, March 11, 2014 Sheet 12 of 57



Memory SO-Dimm CH B

12X021893000

9 M_CHB_MAA[0..15] >>> M_CHB_DQ[0..63] 9

0~7 8~15 16~23 24~31 32~39 40~47 48~55 56~63

13.26.29.30.44 SMB_CLK_S
13.26.29.30.44 SMB_DAT_S

DDR3_DIMM_204P
H:4.0mm

place the cap near to dimm reset pin

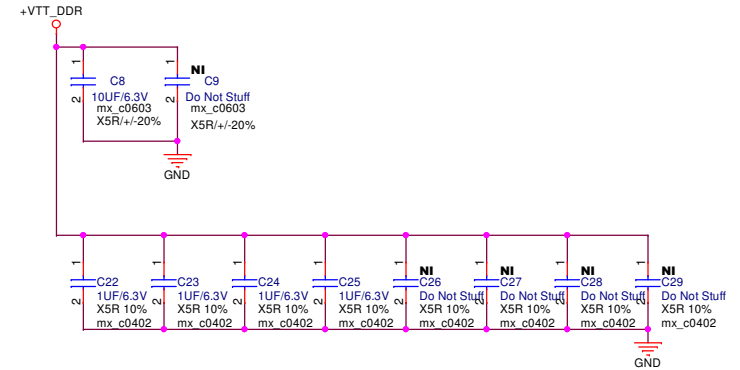
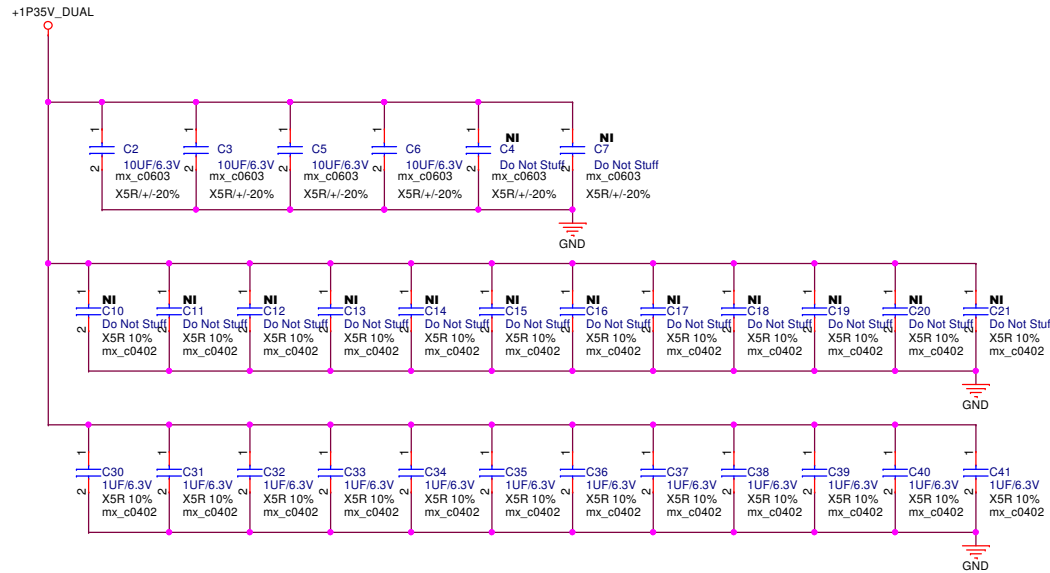
1.01FINAL

PEGATRON Title : SO-DIMM
PEGATRON COMPUTER INC Engineer: Stonko_Chen

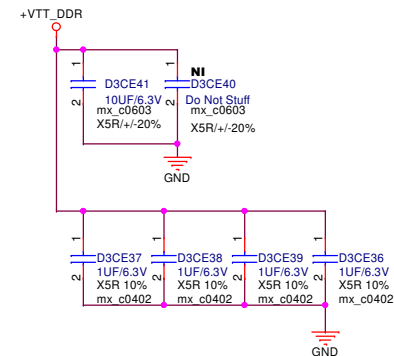
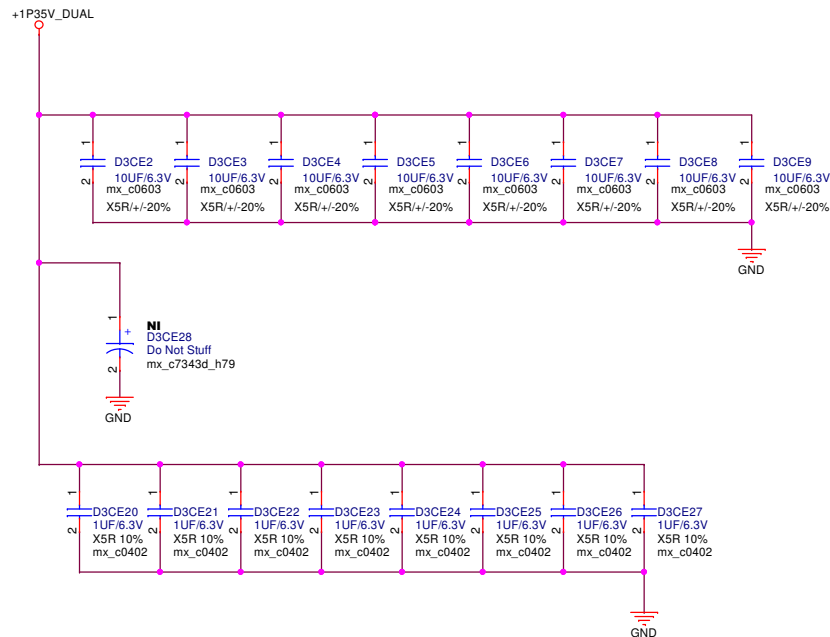
Size	Project Name	Rev
A3	IMPBW-CS	A00

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DDR3L MEMORY DOWN CHANNEL-A PDBOM



DDR3L SODIMM CHANNEL-B PDBOM



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3L-RS_Decoupling

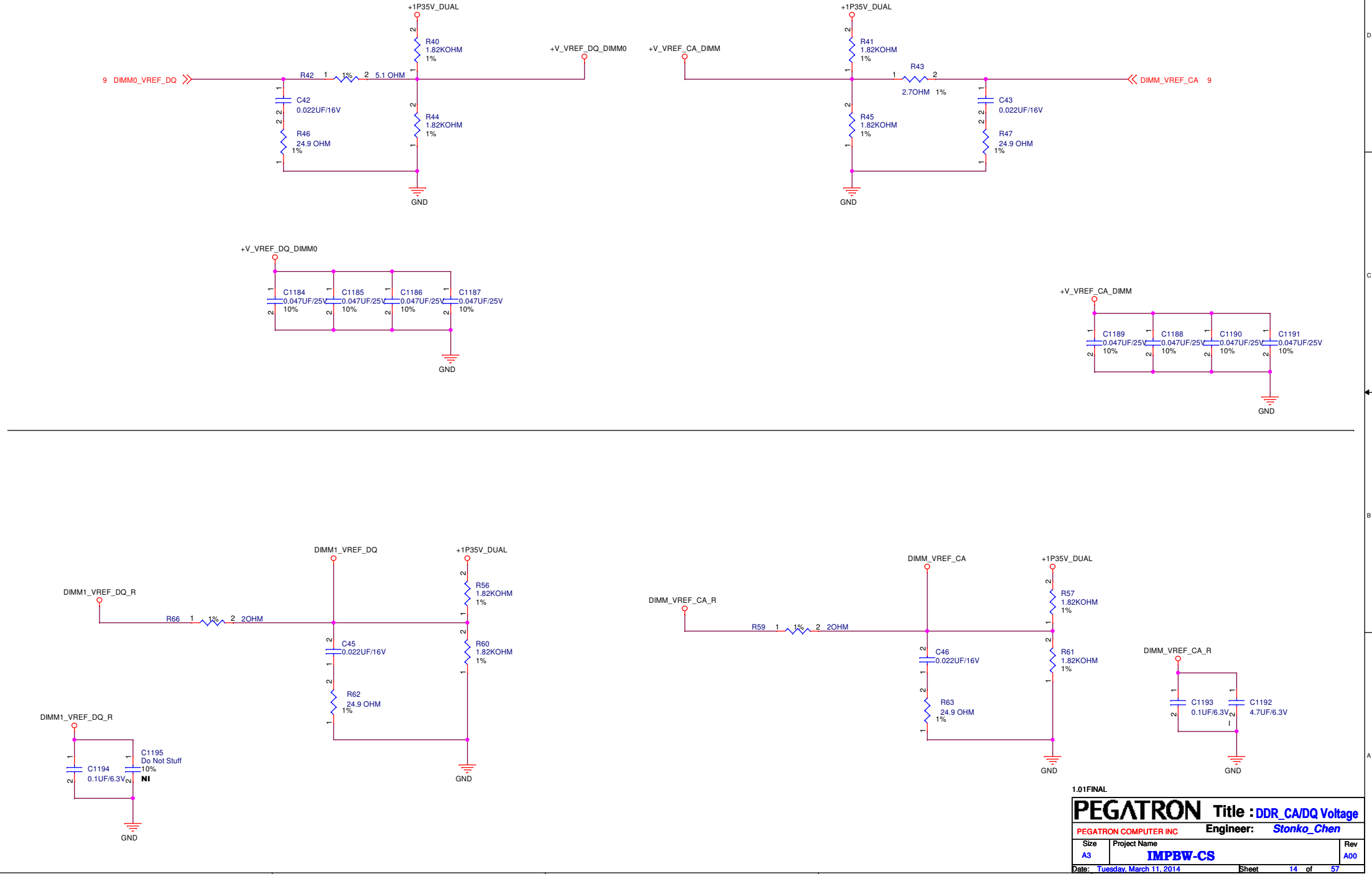
PEGATRON COMPUTER INC Engineer: Stonko_Chen

Size A3	Project Name IMPBW-CS	Rev A00
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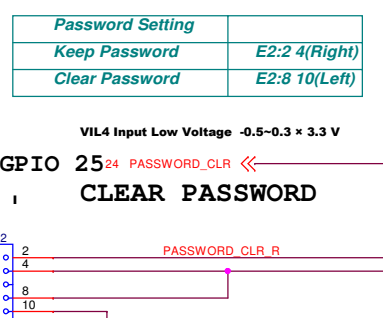
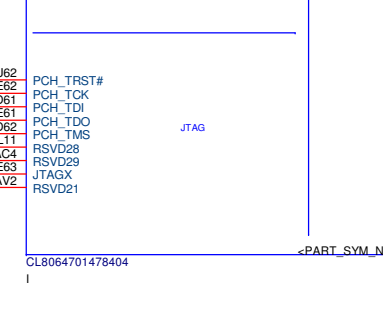
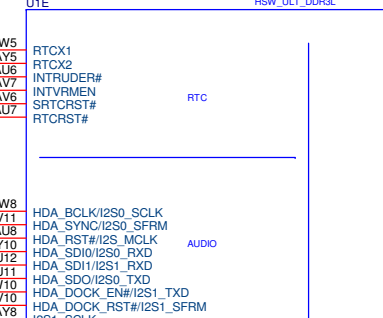
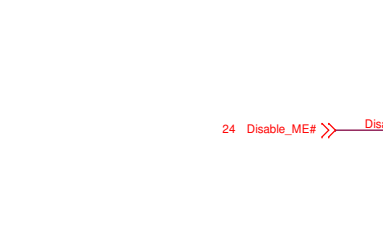
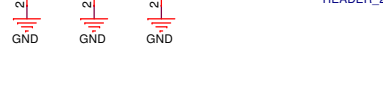
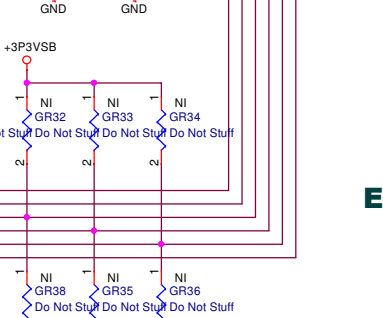
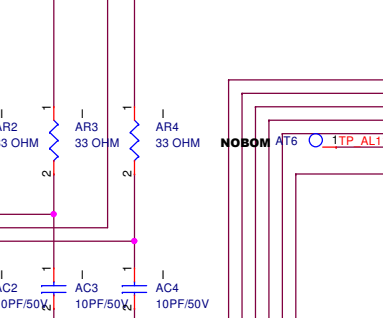
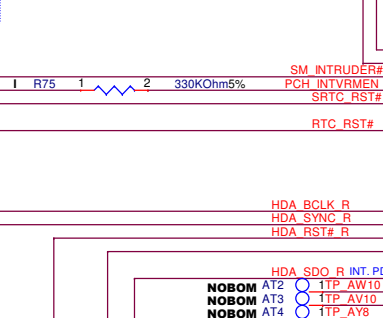
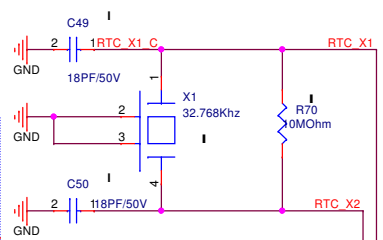
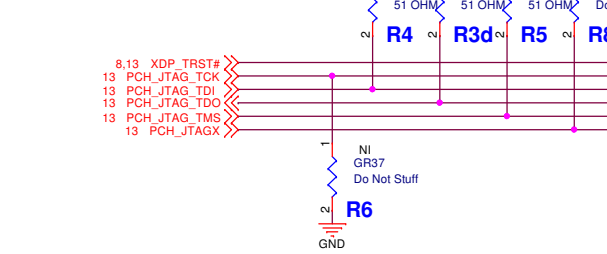
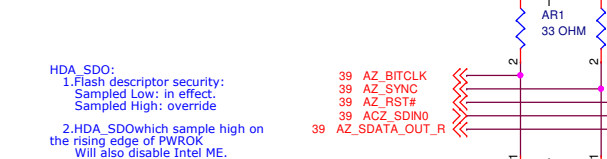
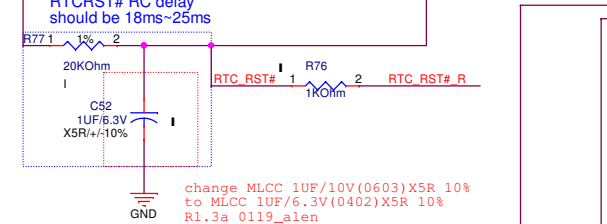
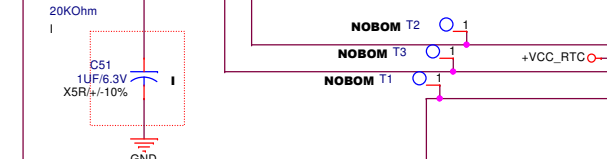
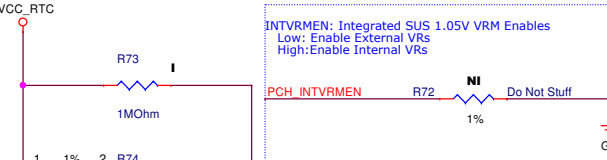
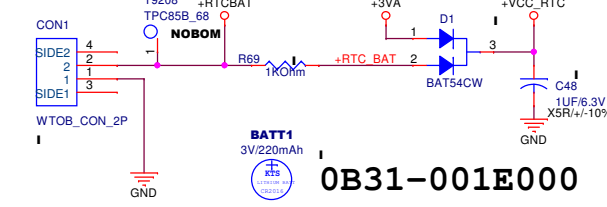
Date: Tuesday, March 11, 2014 Sheet 13 of 57

DDR3L Vref

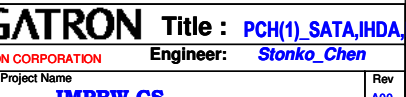
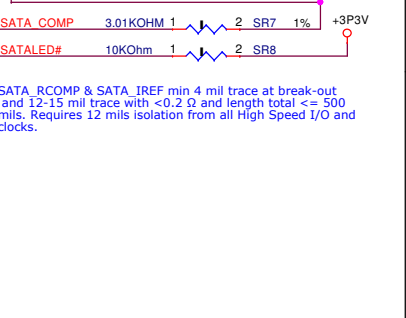
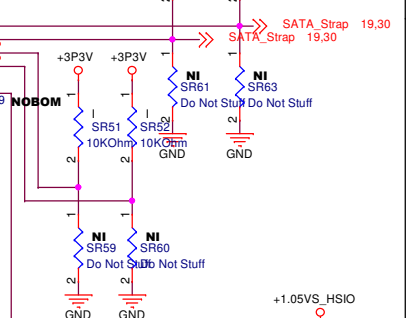
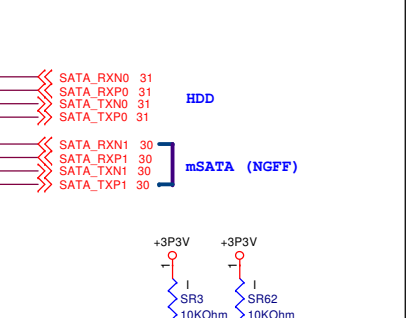
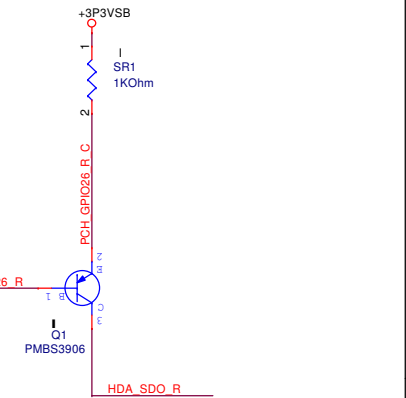
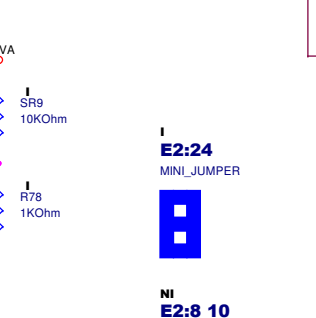
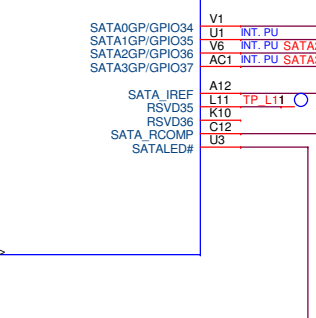
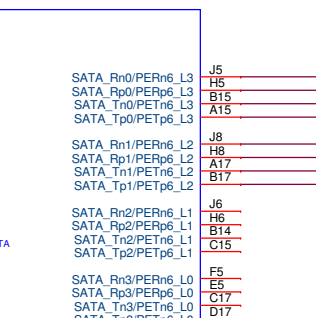
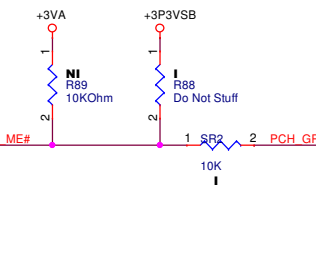
M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off



RTC battery 1217-001M000 替代料件



ACZ_SDOUT:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2.ACZ_SDOUTwhich sample high on the rising edge of PWROK
Will also disable Intel ME.

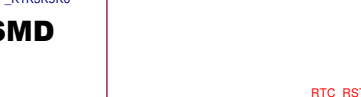
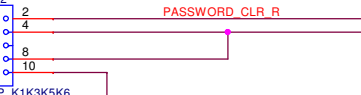


Password Setting	
Keep Password	E2:2 4(Right)
Clear Password	E2:8 10(Left)

VIL4 Input Low Voltage -0.5~0.3 × 3.3 V

GPIO 25²⁴ PASSWORD_CLR

E2 CLEAR PASSWORD



E2:24
MINI_JUMPER

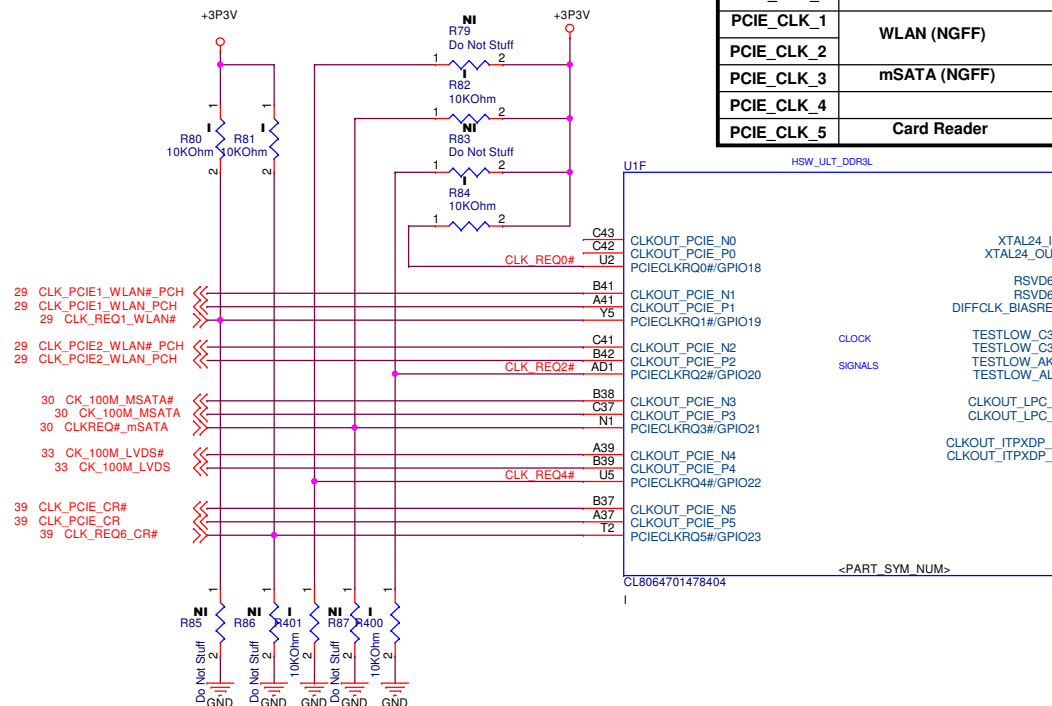


E2:8 10
Do Not Stuff

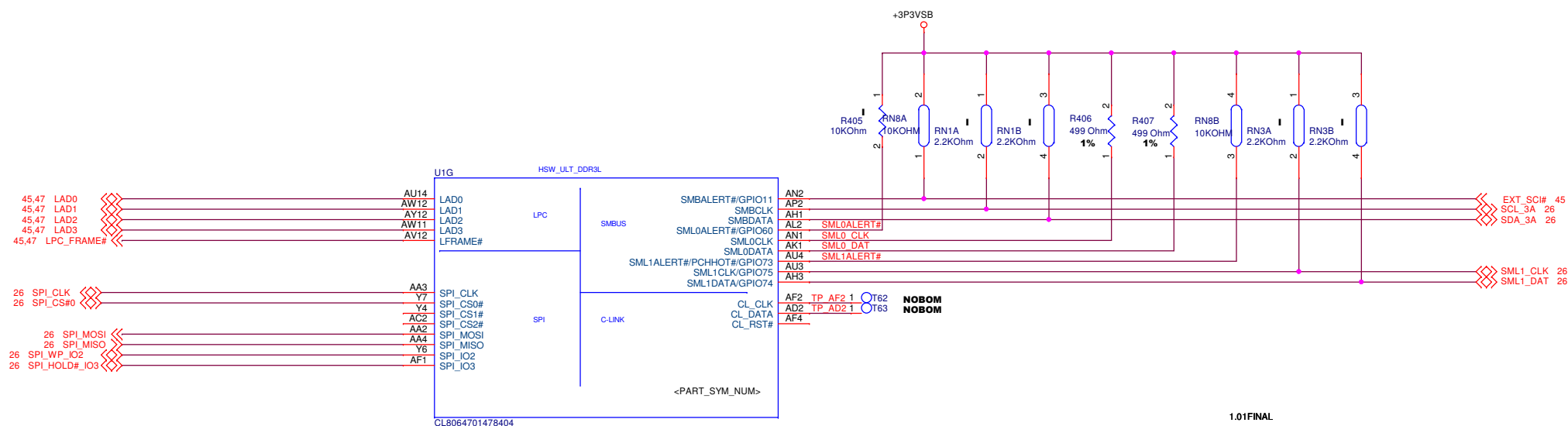
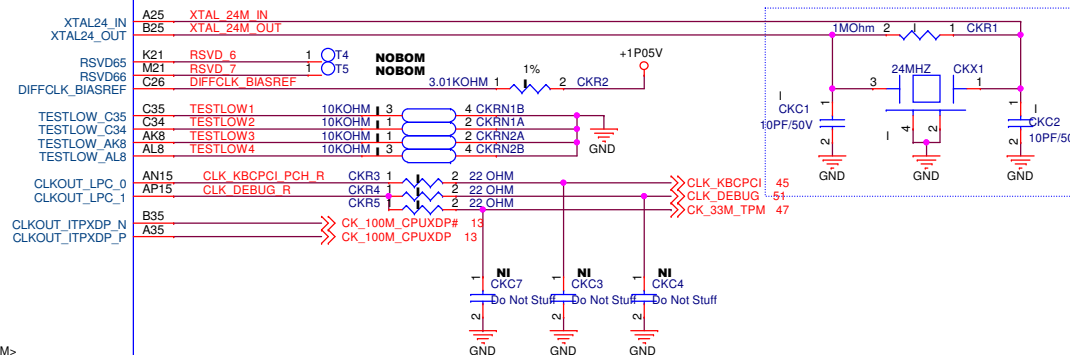


PCH CLKREQ Setting:
Not connected to device.
PCIECLKRQ[5:0]# are core well powered.

PCIE_CLK_0	
PCIE_CLK_1	WLAN (NGFF)
PCIE_CLK_2	
PCIE_CLK_3	mSATA (NGFF)
PCIE_CLK_4	
PCIE_CLK_5	Card Reader



24-MHz is required



PEGATRON Title : PCH(2)_PCIE,CLK,SMB,I

PEGATRON CORPORATION		Engineer:	Stonko_Chen
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CARD READER

39 PCIE_RXN6_CR
39 PCIE_RXP6_CR
39 PCIE_TXN6_CR
39 PCIE_TXP6_CR

PCIE 1	
PCIE 2	
PCIE 3	
PCIE 4	NGFF Card (WLAN)
PCIE 5	Card Reader
PCIE 6	

WLAN

29 PCIE_RXN3_WLAN
29 PCIE_RXP3_WLAN
29 PCIE_TXN3_WLAN
29 PCIE_TXP3_WLAN

29 PCIE_RXN4_WLAN
29 PCIE_RXP4_WLAN
29 PCIE_TXN4_WLAN
29 PCIE_TXP4_WLAN

+1.05VS_AUSB3PLL

NOBOM ST1 1 TP E15 E15
NOBOM ST2 1 TP E13 E13
SR10 1 3.01KOHM PCIE_RCOMP
A27
B27
PCIE_IREF

U1K HSW_ULT_DDR3L
F10 PERn5_L0
E10 PERp5_L0
C23 PETn5_L0
C22 PETp5_L0
F8 PERn5_L1
E8 PERp5_L1
B23 PETn5_L1
A23 PETp5_L1
H10 PERn5_L2
G10 PERp5_L2
B21 PETn5_L2
C21 PETp5_L2
E6 PERn5_L3
F6 PERp5_L3
B22 PETn5_L3
A21 PETp5_L3
G11 PERn3
F11 PERp3
C29 PETn3
B30 PETp3
F13 PERn4
G13 PERp4
B29 PETn4
A29 PETp4
G17 PERn1/USB3Rn3
F17 PERp1/USB3Rp3
C30 PETn1/USB3Tn3
C31 PETp1/USB3Tp3
F15 PERn2/USB3Rn4
G15 PERp2/USB3Rp4
B31 PETn2/USB3Tn4
A31 PETp2/USB3Tp4
RSVD26
RSVD27
PCIE_RCOMP
PCIE_IREF
CL8064701478404

PCIE

USB

USB2n0 AN8
USB2p0 AM8
USB2n1 AR7
USB2p1 AT7
USB2n2 AR8
USB2p2 AP8
USB2n3 AR10
USB2p3 AT10
USB2n4 AM15
USB2p4 AL15
USB2n5 AM13
USB2p5 AN13
USB2n6 AP11
USB2p6 AN11
USB2n7 AR13
USB2p7 AP13
USB3Rn1 G20
USB3Rp1 H20
USB3Tn1 C33
USB3Tp1 B34
USB3Rn2 E18
USB3Rp2 F18
USB3Tn2 B33
USB3Tp2 A33
USB3BIAS# AJ10
USB3BIAS AJ11
RSVD50 AN10
RSVD51 AM10
OC0#/GPIO40 AL3
OC1#/GPIO41 AT1
OC2#/GPIO42 AH2
OC3#/GPIO43 AV3

USB_PN0 39
USB_PP0 39
USB_PN1 39
USB_PP1 39
USB_PN2 38
USB_PP2 38
USB_PN3 37
USB_PP3 37
USB_PN4 39
USB_PP4 39
USB_PN5 42
USB_PP5 42
USB_PN6 29
USB_PP6 29
USB_PN7 30
USB_PP7 30
USB3_RXN0 36
USB3_RXP0 36
USB3_TXN0 36
USB3_TXP0 36
USB3_RXN1 36
USB3_RXP1 36
USB3_TXN1 36
USB3_TXP1 36

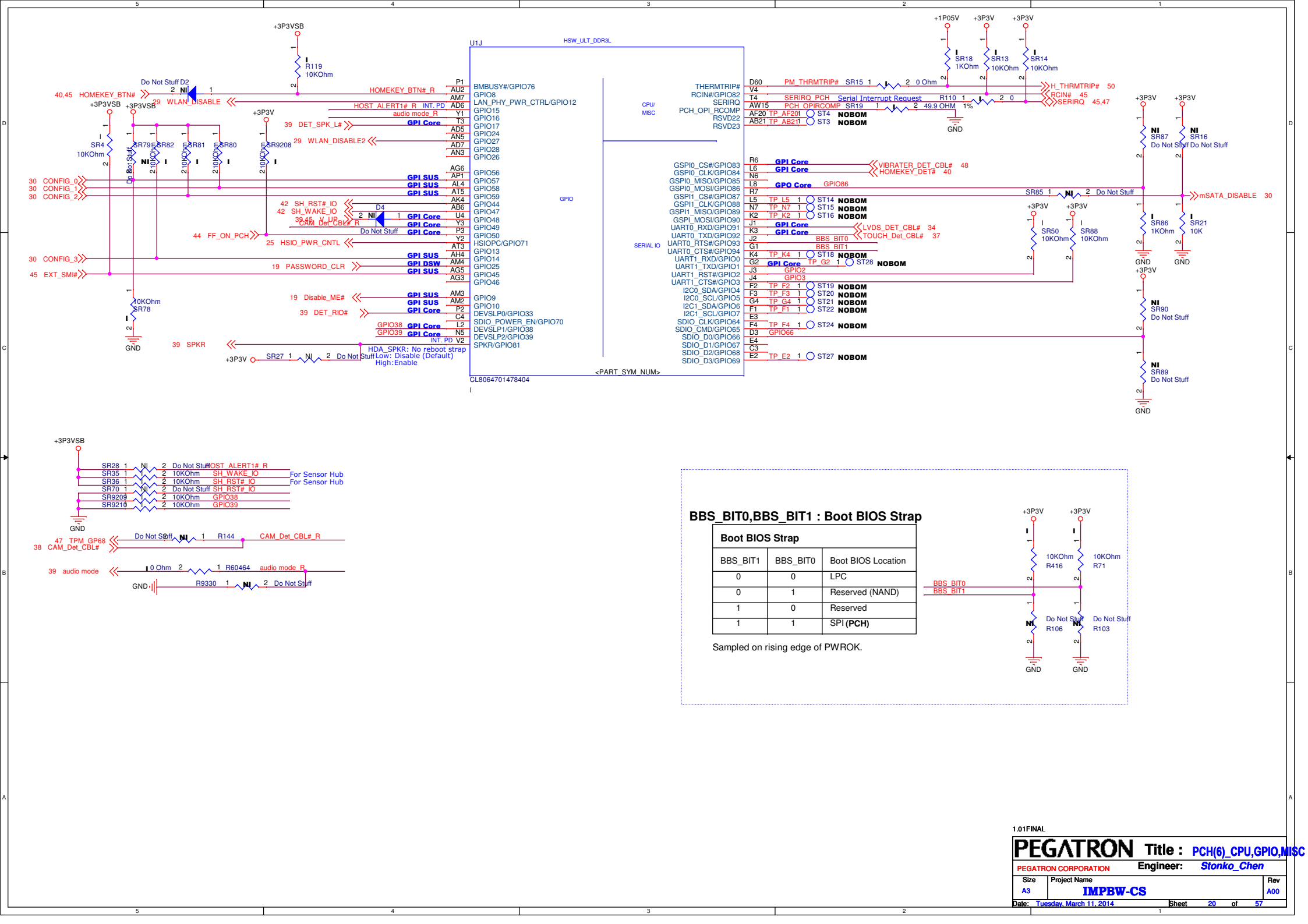
USB2.0 port - Combo with USB3.0-R
USB2.0 port - Combo with USB3.0-L
Camera
Touch Screen
USB2.0 port RF
Sensor Hub
WiFi
mSATA

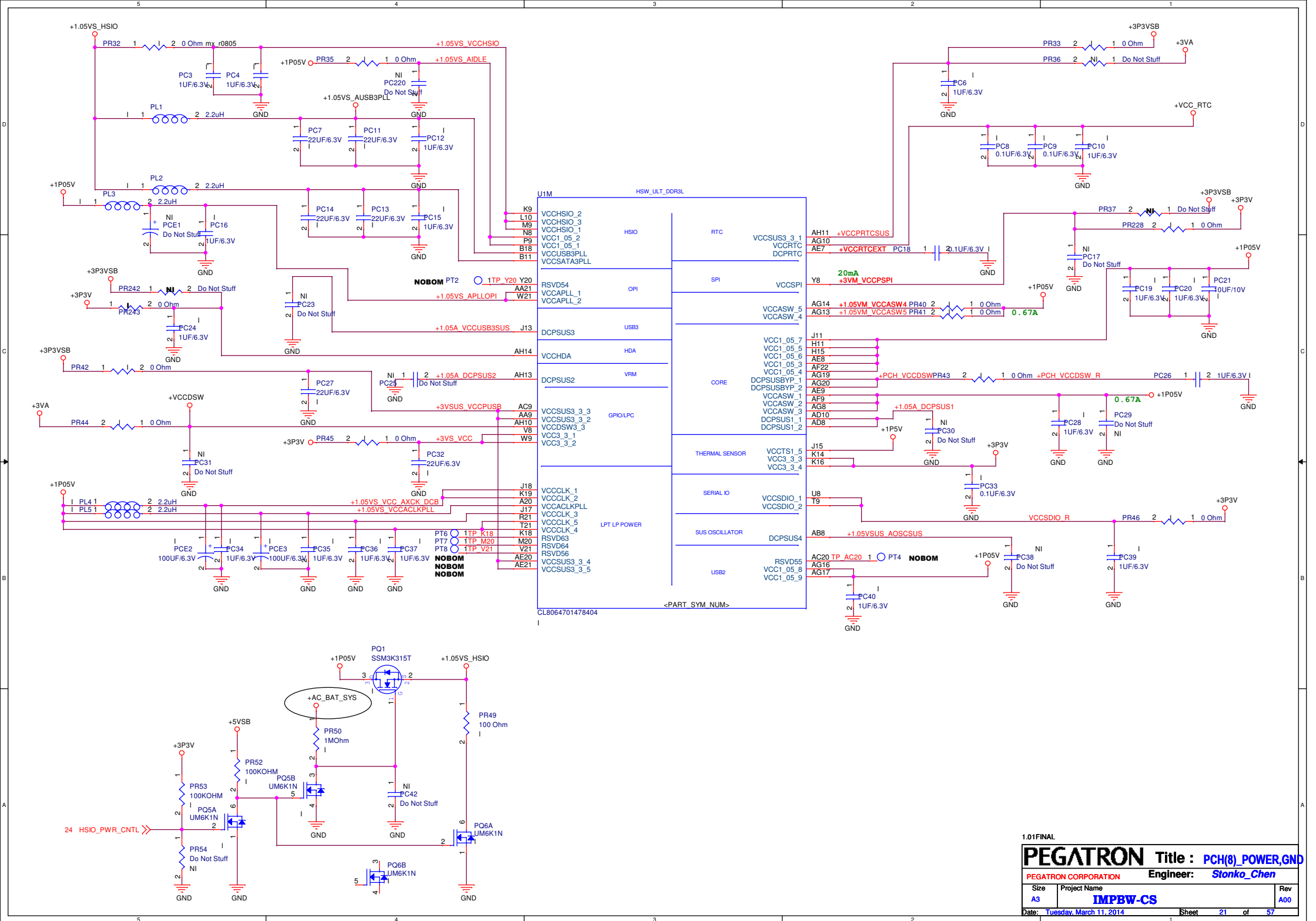
USBCOMP (R2403): TIE TRACES TOGETHER CLOSE TO PINS, WITH LENGTH NO LONGER THAN 450 MILS TO RESISTOR

USB_BIAS R108 1 1% 22.6 OHM
GND

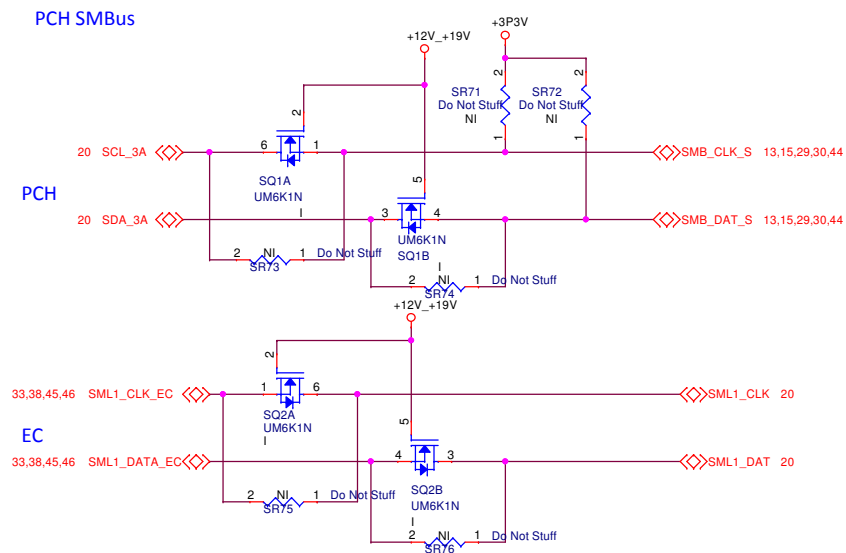
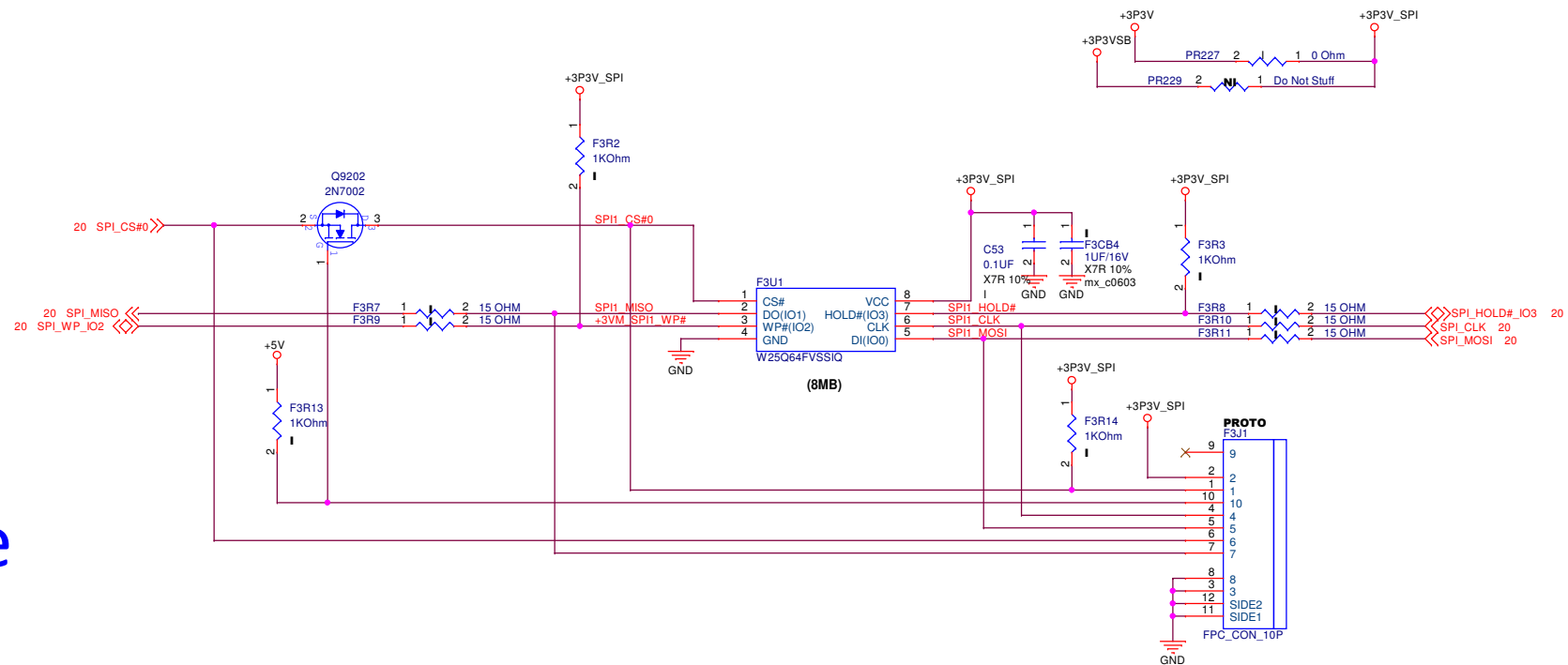
+3P3VSB
R109 10KOhm

1.01FINAL



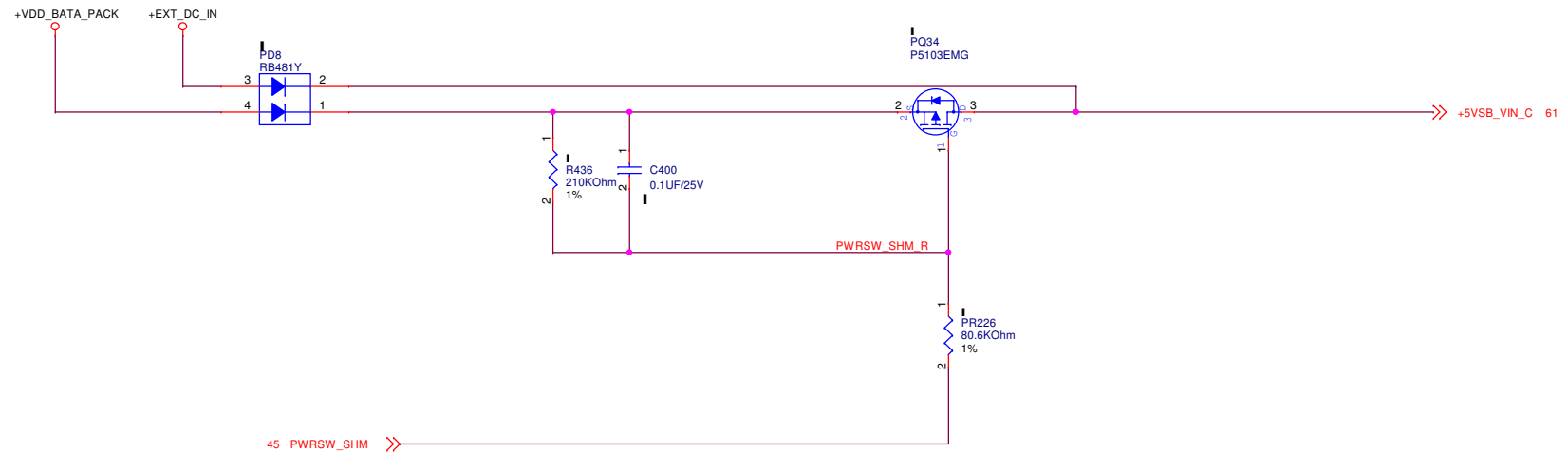


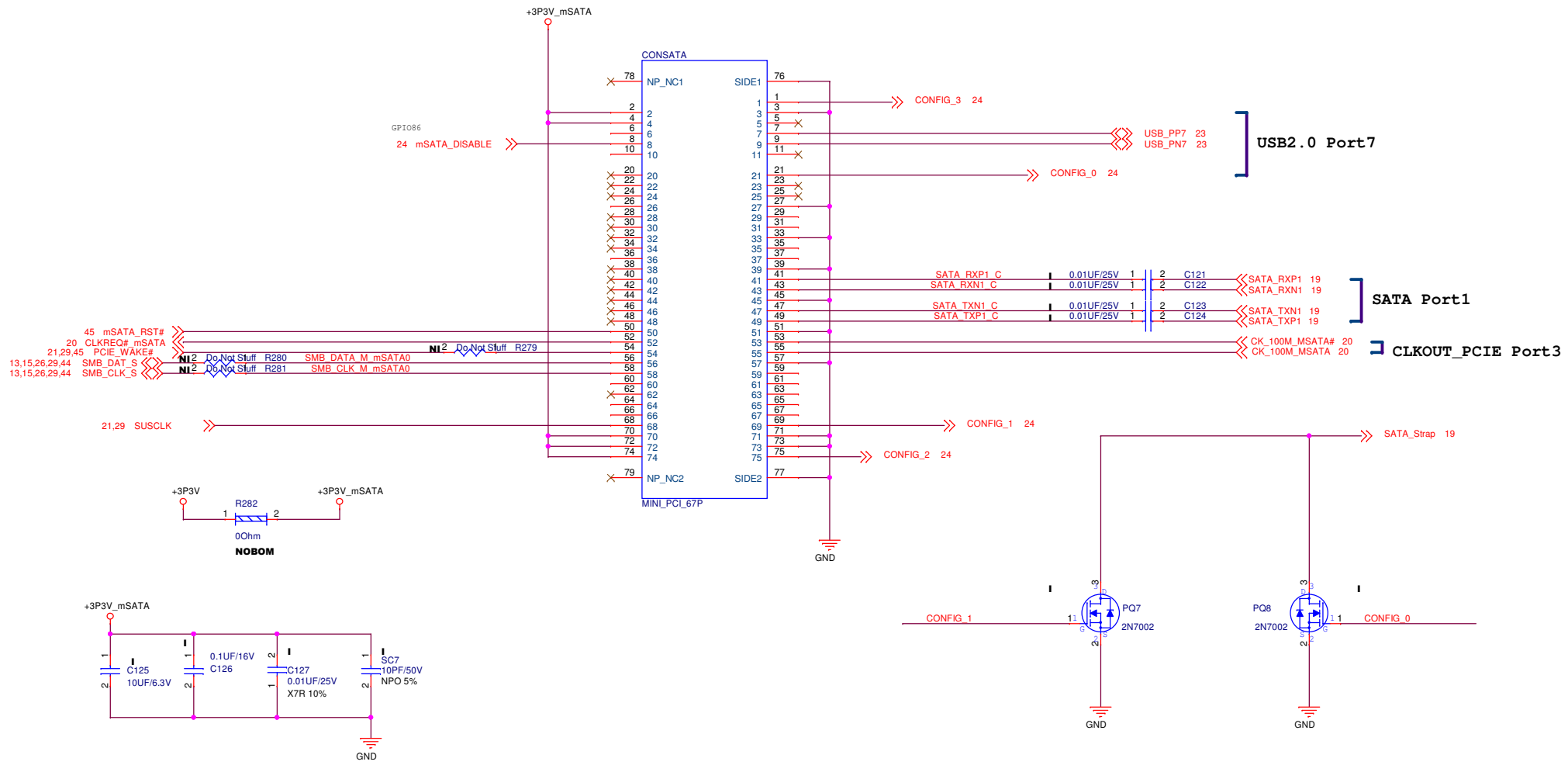
lack of diode

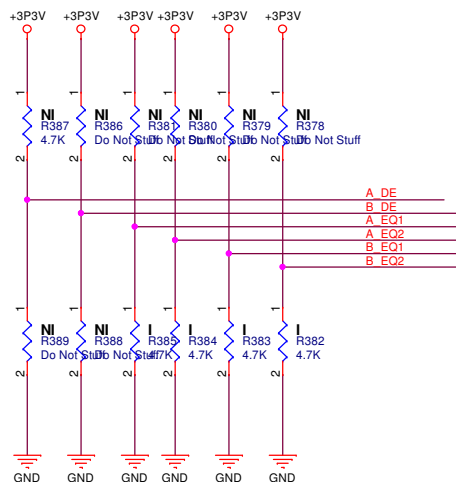
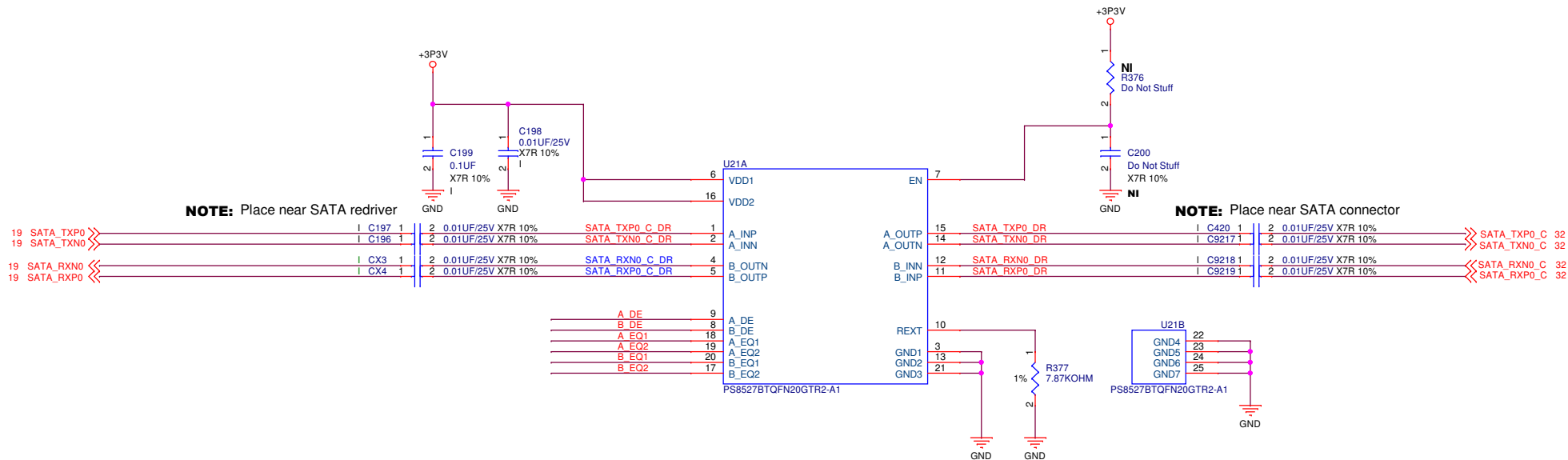


SMBUS Link device

- CPU XDP
- DIMM
- PCIE mini Card
- FFS G-SENSOR





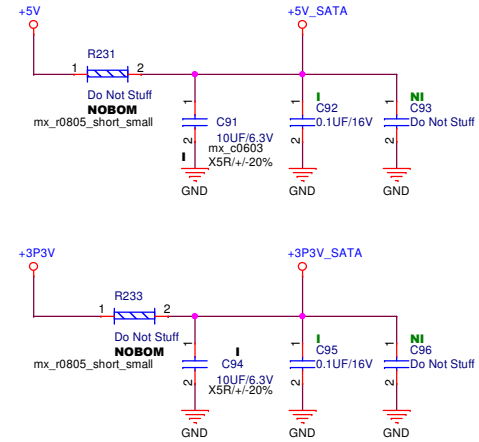
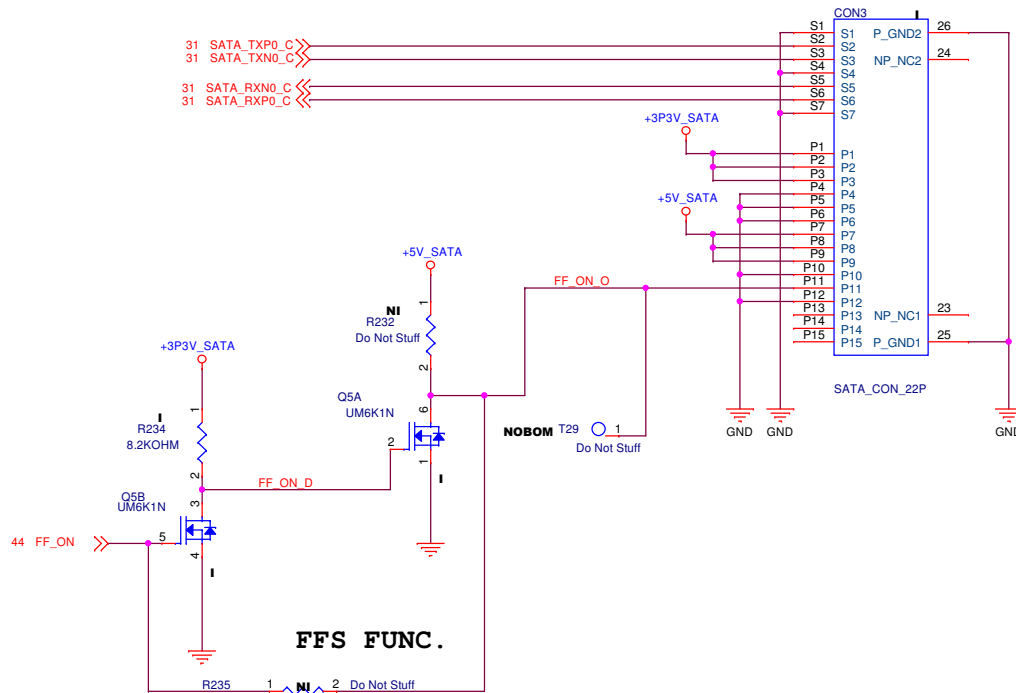


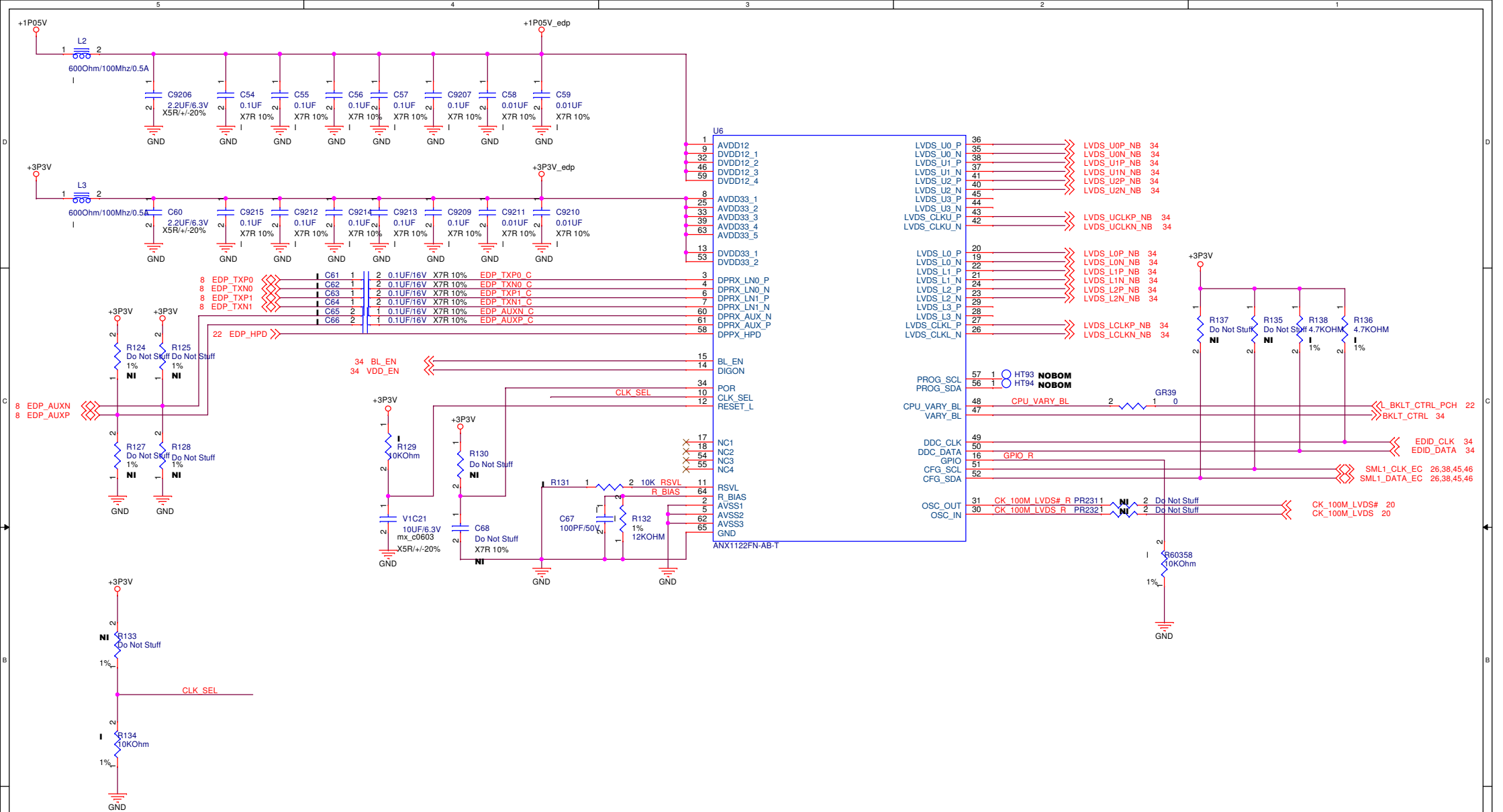
A/B_EQ2	A/B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

A/B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-1.5dB

1.01FINAL

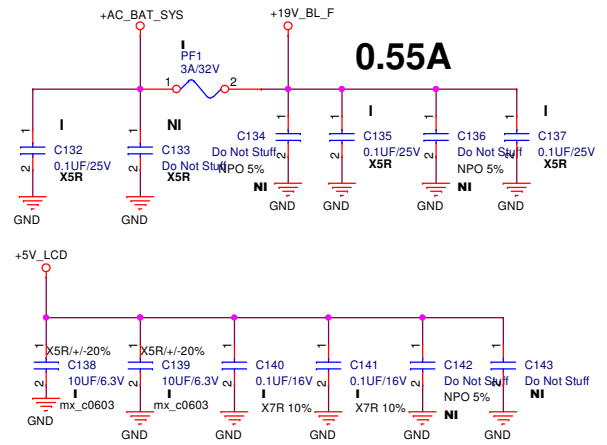
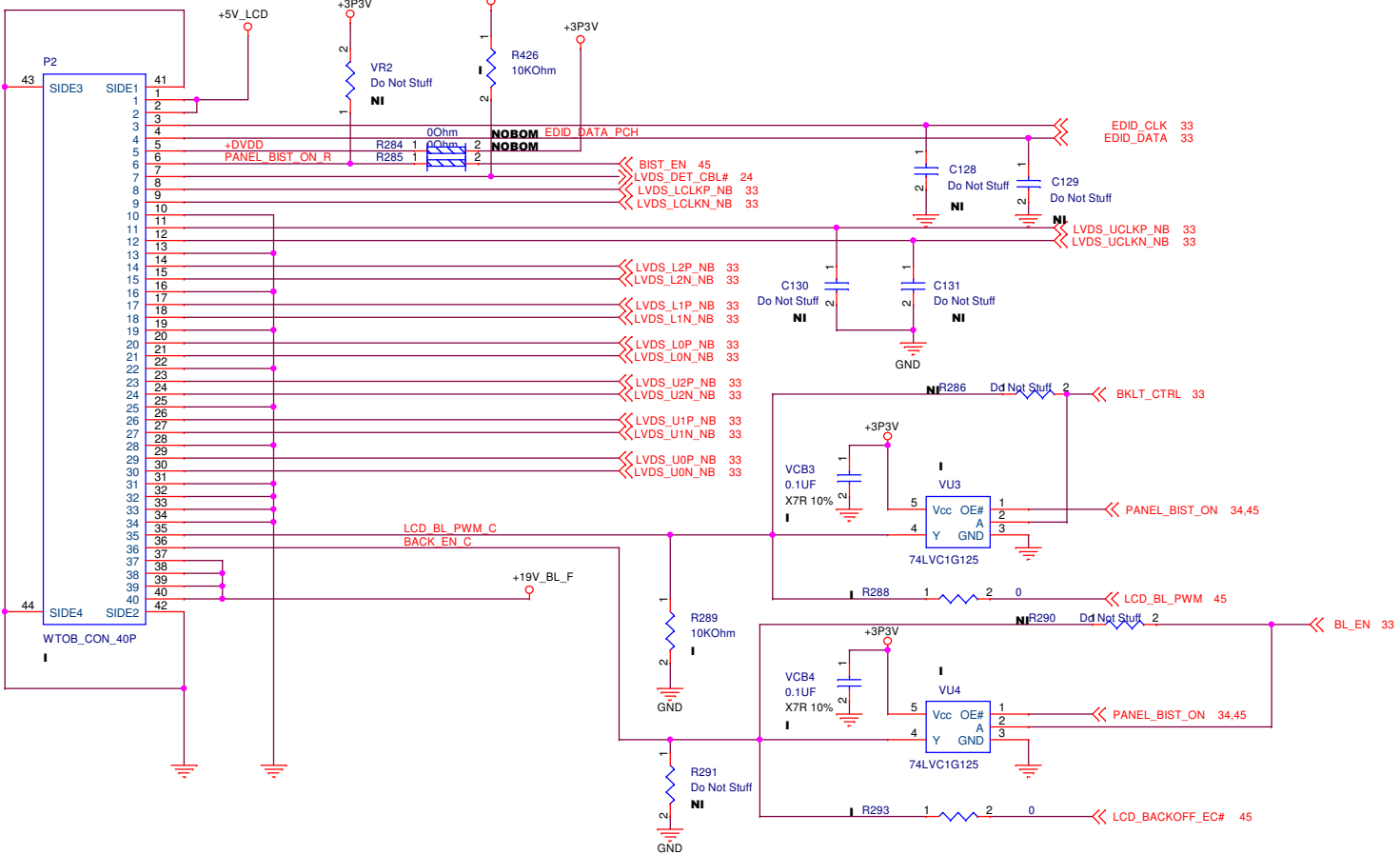
SATA HDD



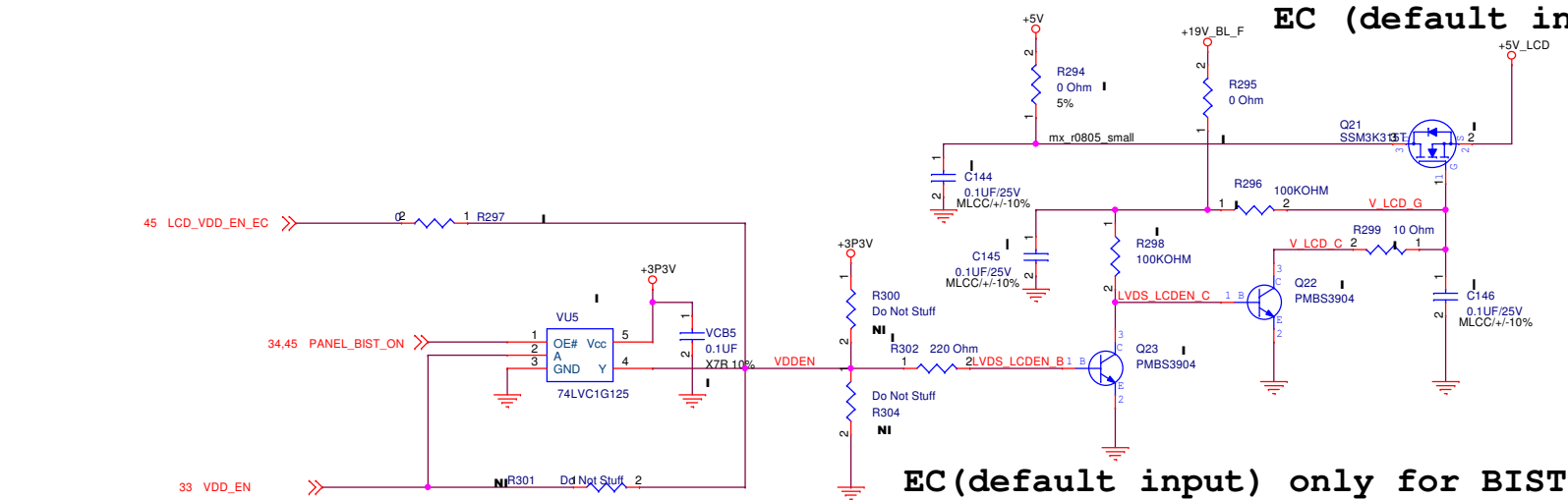


Input CLK selection
 Pull up: work with 100M clock from Pin 30/31.
 Pull down: work with on chip OSC and Pin 30/31 leave it as floating pin

LVDS



EC (default input) only for BIST



USB 3.0 redriver

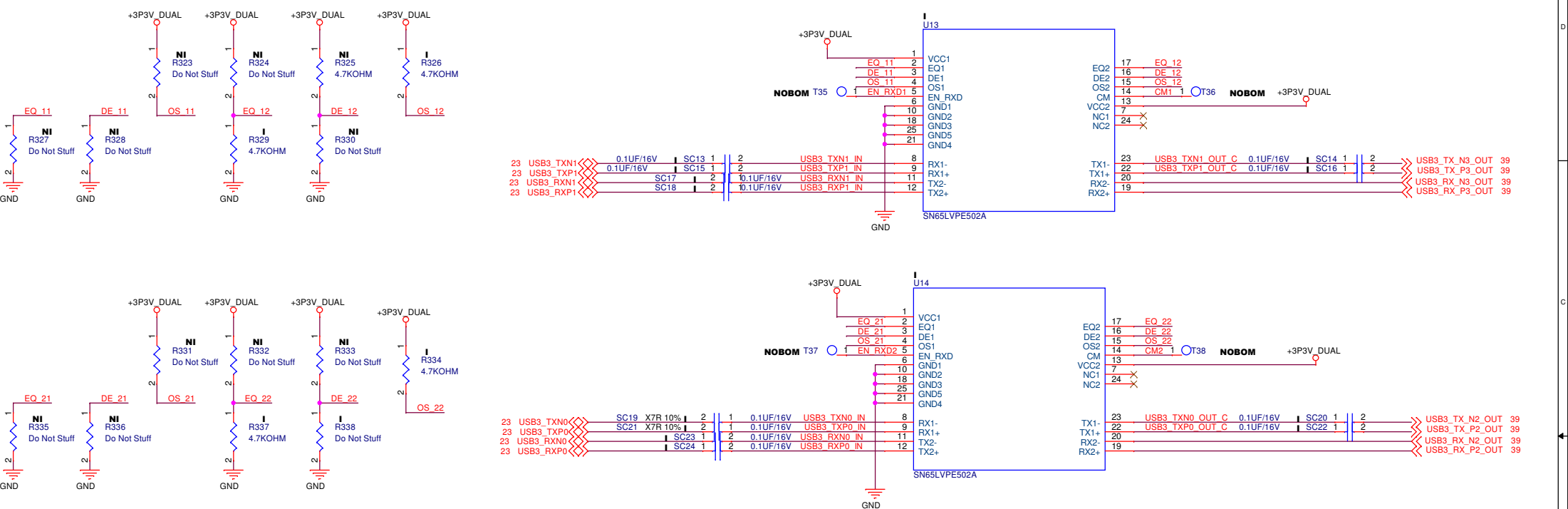
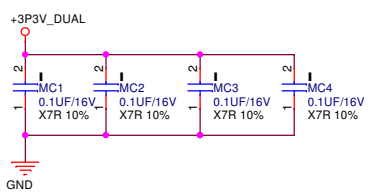
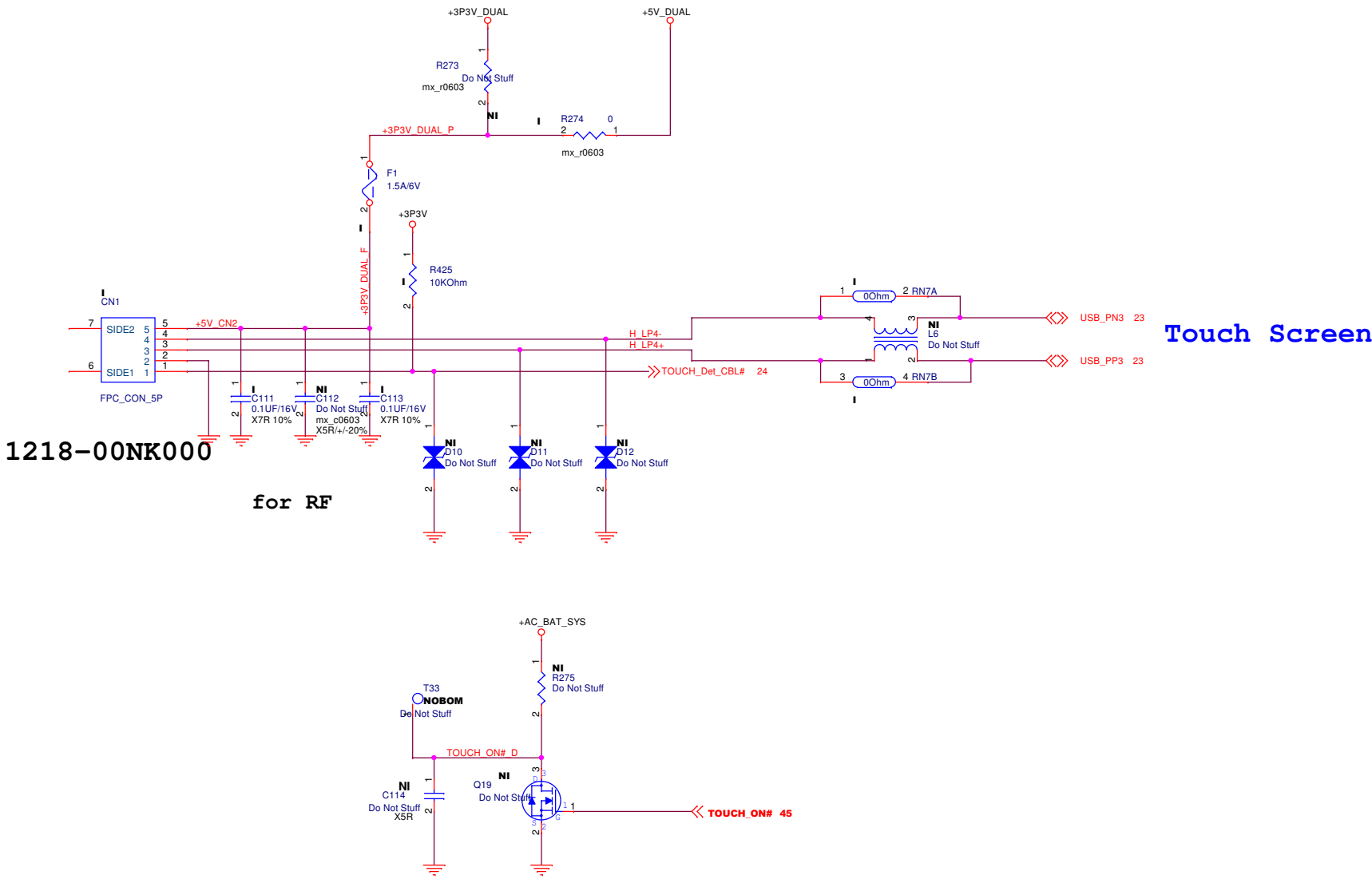


Table 2. Signal Control Pin Setting

OUTPUT SWING AND EQ CONTROL (at 2.5 GHz)			
OS _x ⁽¹⁾	TRANSISTION BIT AMPLITUDE (TYP mVpp)	EQ _x ⁽¹⁾	EQUALIZATION (dB)
NC (default)	1042	NC (default)	0
0	908	0	7
1	1127	1	15
OUTPUT DE CONTROL (at 2.5 GHz)			
DE _x ⁽¹⁾	OS _x ⁽¹⁾ = NC	OS _x ⁽¹⁾ = 0	OS _x ⁽¹⁾ = 1
NC (default)	0 dB	0 dB	0 dB
0	-3.5 dB	-2.2 dB	-4.4 dB
1	-6.0 dB	-5.2 dB	-6.0 dB
CONTROL PINS SETTINGS			
EN_RXD	DEVICE FUNCTION	CM	DEVICE FUNCTION
1 (default)	Normal Operation	0 (default)	Normal Operation
0	Sleep Mode	1	Compliance Test Mode



TOUCH

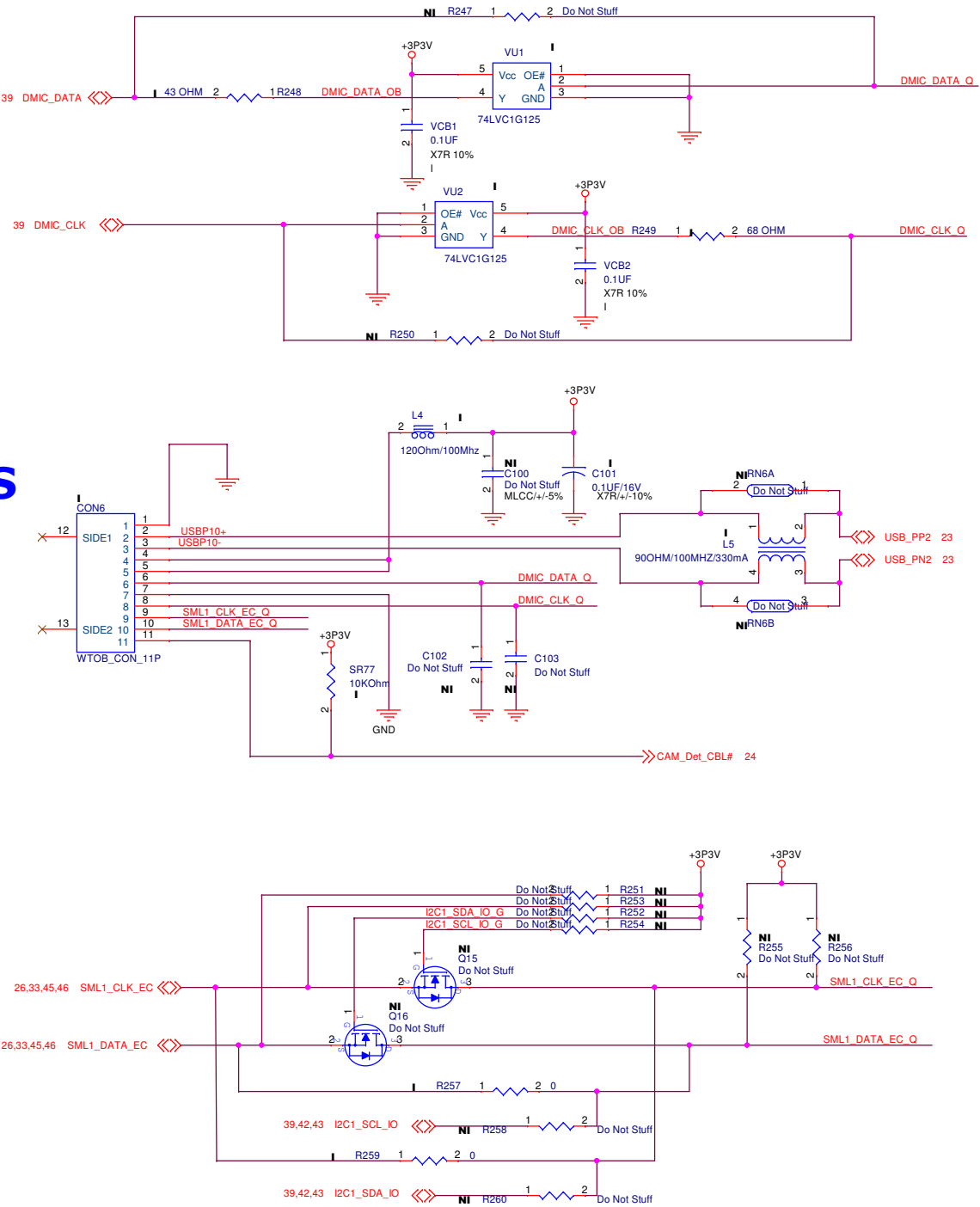


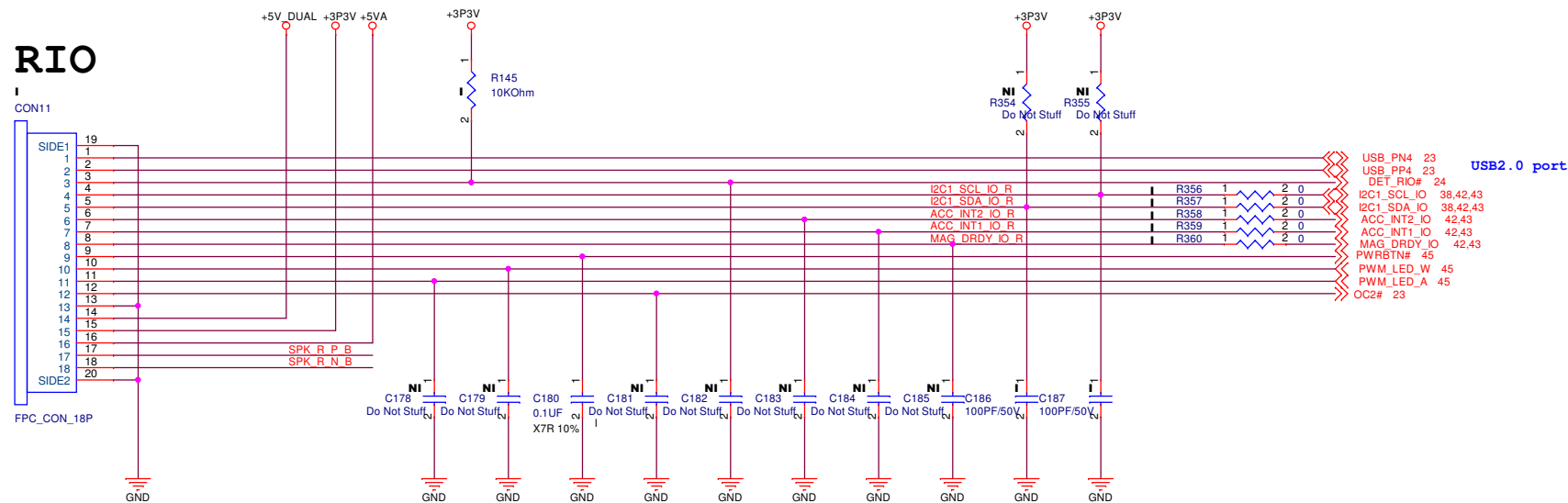
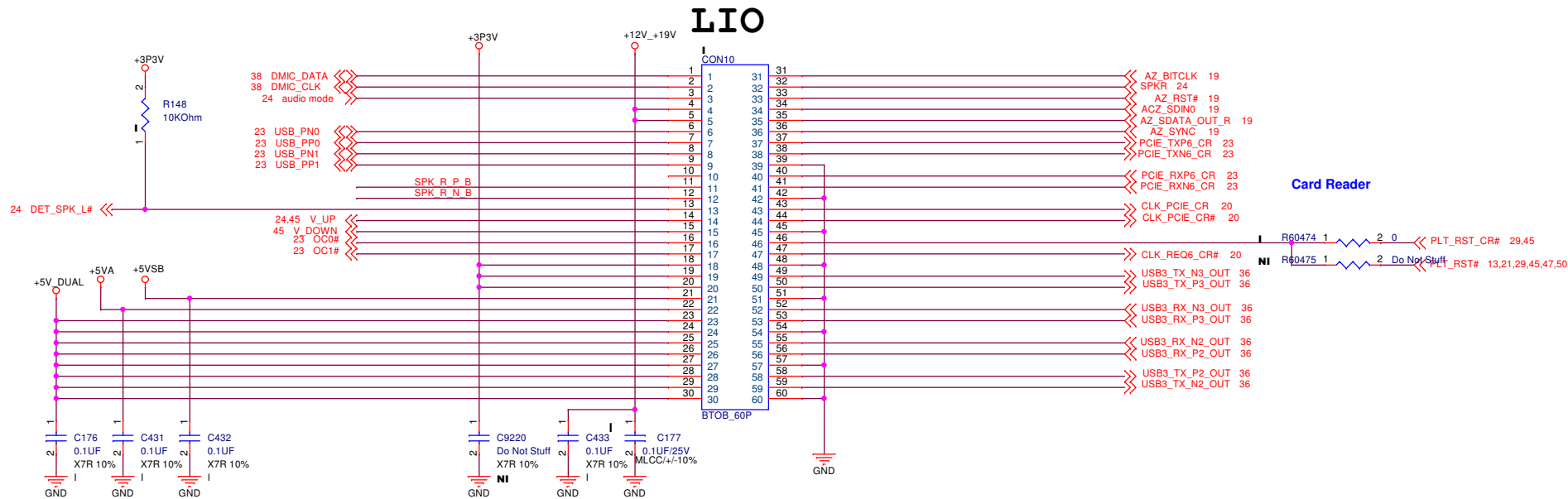
Camera Module & DMIC & ALS

Digital MIC

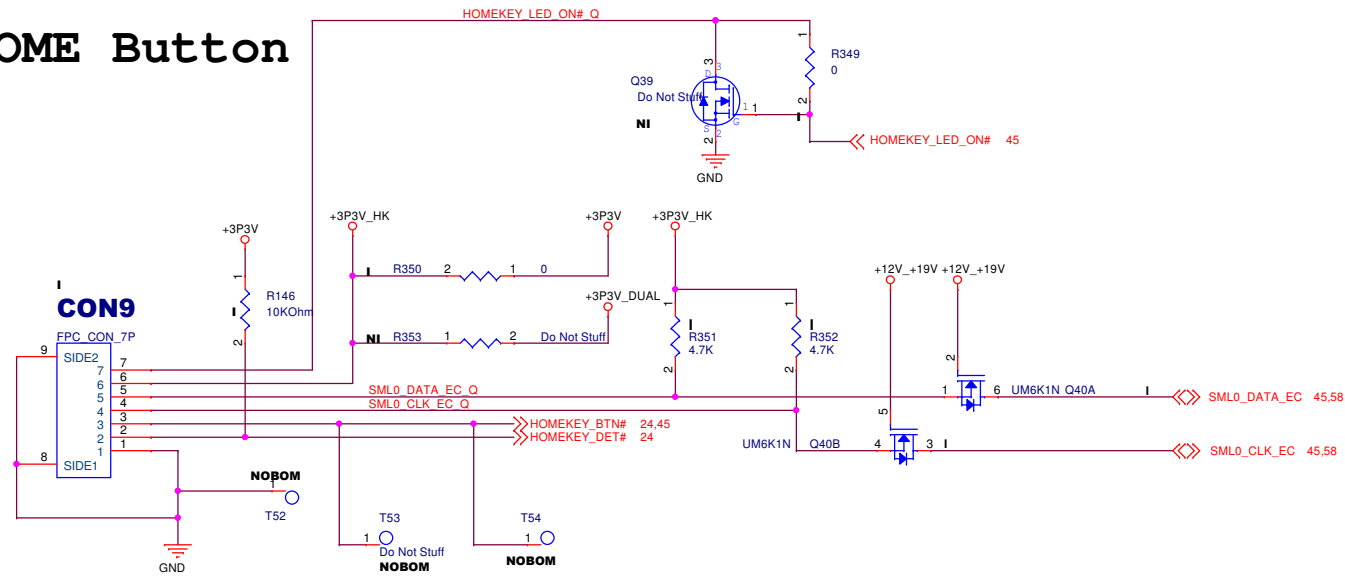
CAMERA

ALS





HOME Button



1.01FINAL

PEGATRON		Title :	Homekey_connector
PEGATRON COMPUTER INC		Engineer:	Stonko_Chen
Size	Project Name		Rev
A3	IMPBW-CS		A00
Date: Tuesday, March 11, 2014		Sheet	34 of 57

Sensor Hub - IT8350E

Layout Notice

1. For the ADC layout notice circuits,
 - a) Keep the trace away from Power, fast data bus, and CRTs. Especially PWM DC-DC control.
 - b) Isolate Analog and Digital ground plane.

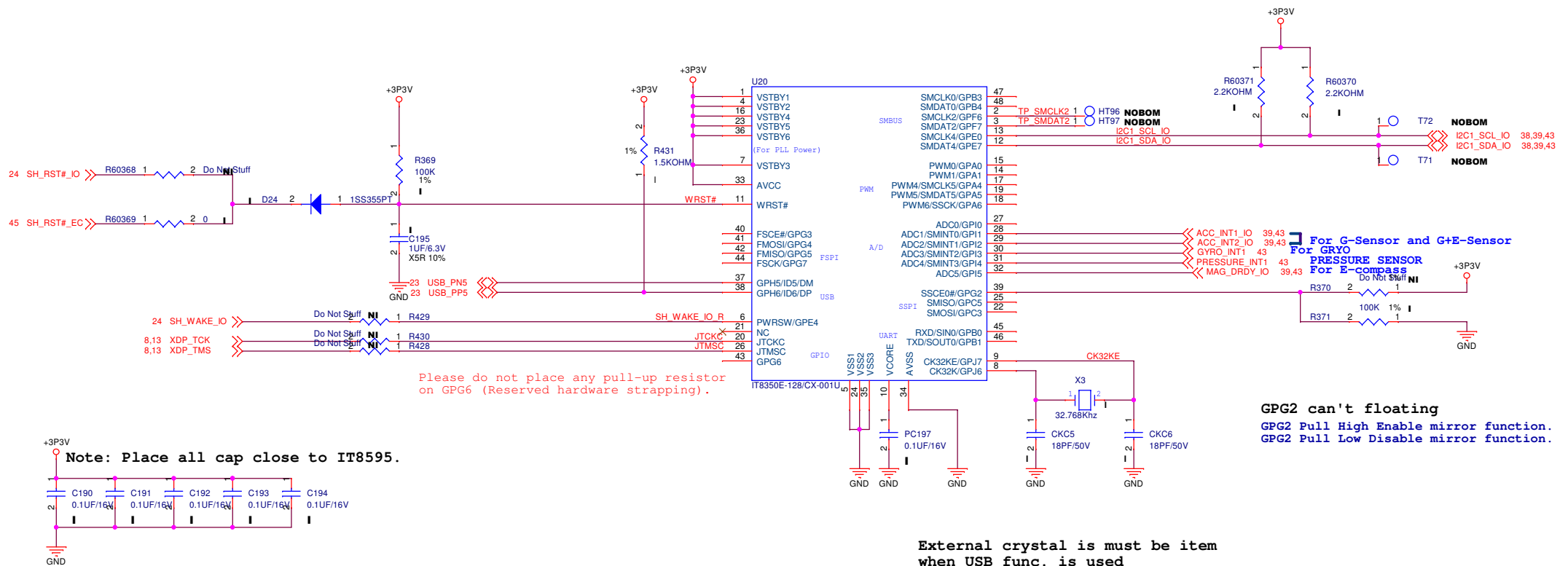
*Recommended net "VSTBY" minimum trace width 12mils.

Note 1 :

Since all GPIO belong to VSTBY power domain

Note 2 :

- (1) Each input pin should be driven or pulled.
- (2) Each output-drain output pin should be pulled.

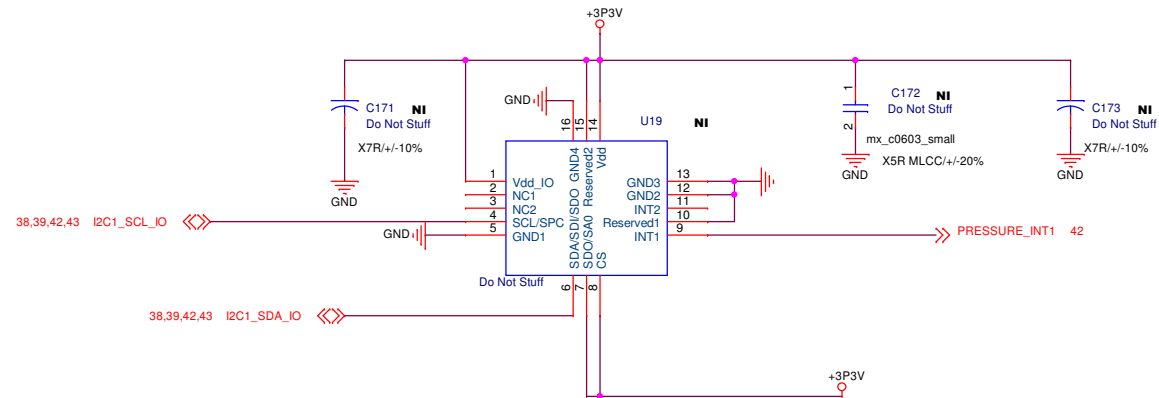


External crystal is must be item
when USB func. is used

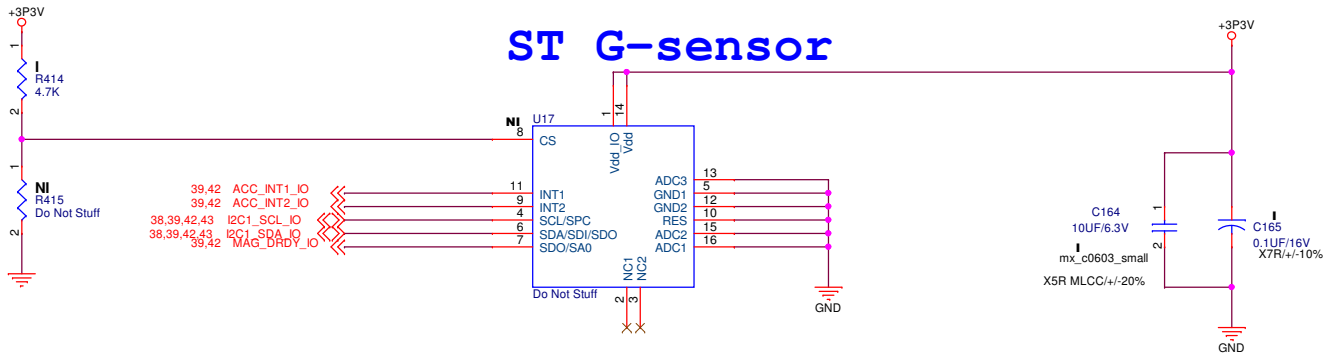
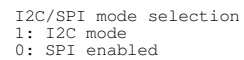
```
32.768kHz clock lines:(for USB must use external crystal)
```

- If possible, please avoid using any through-hole.
- Please make the trace length short, and the trace width wide enough.
- The spacing to the closest neighbor should be wide enough.

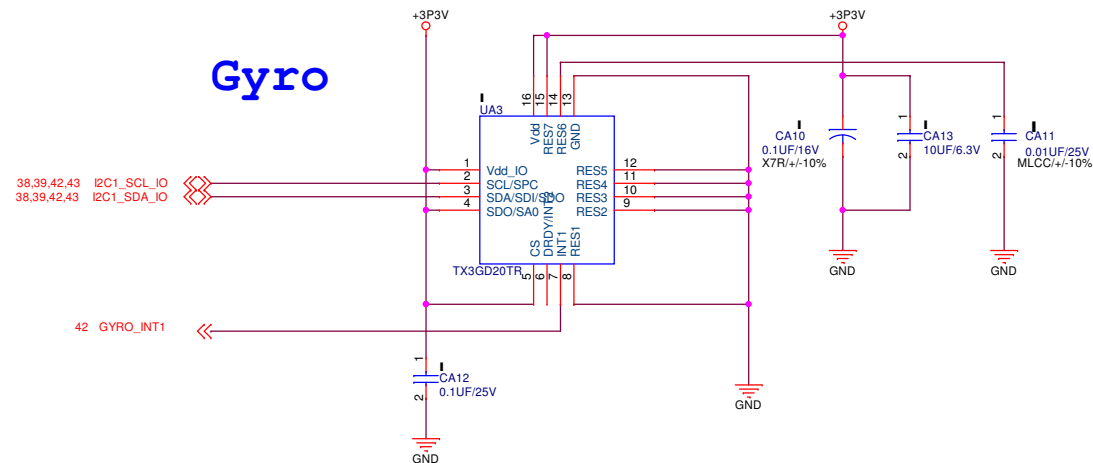
PRESSURE SENSOR



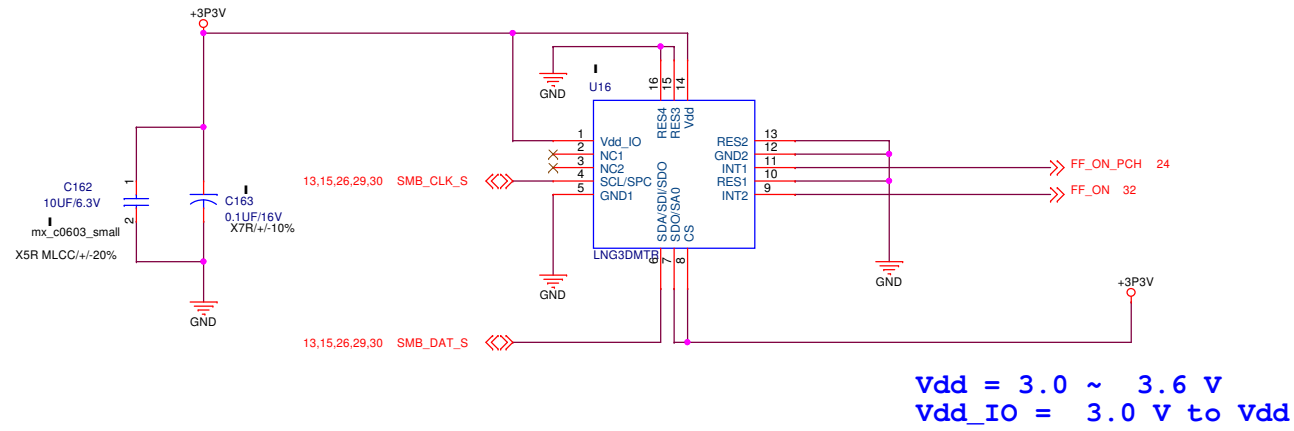
ST G-sensor

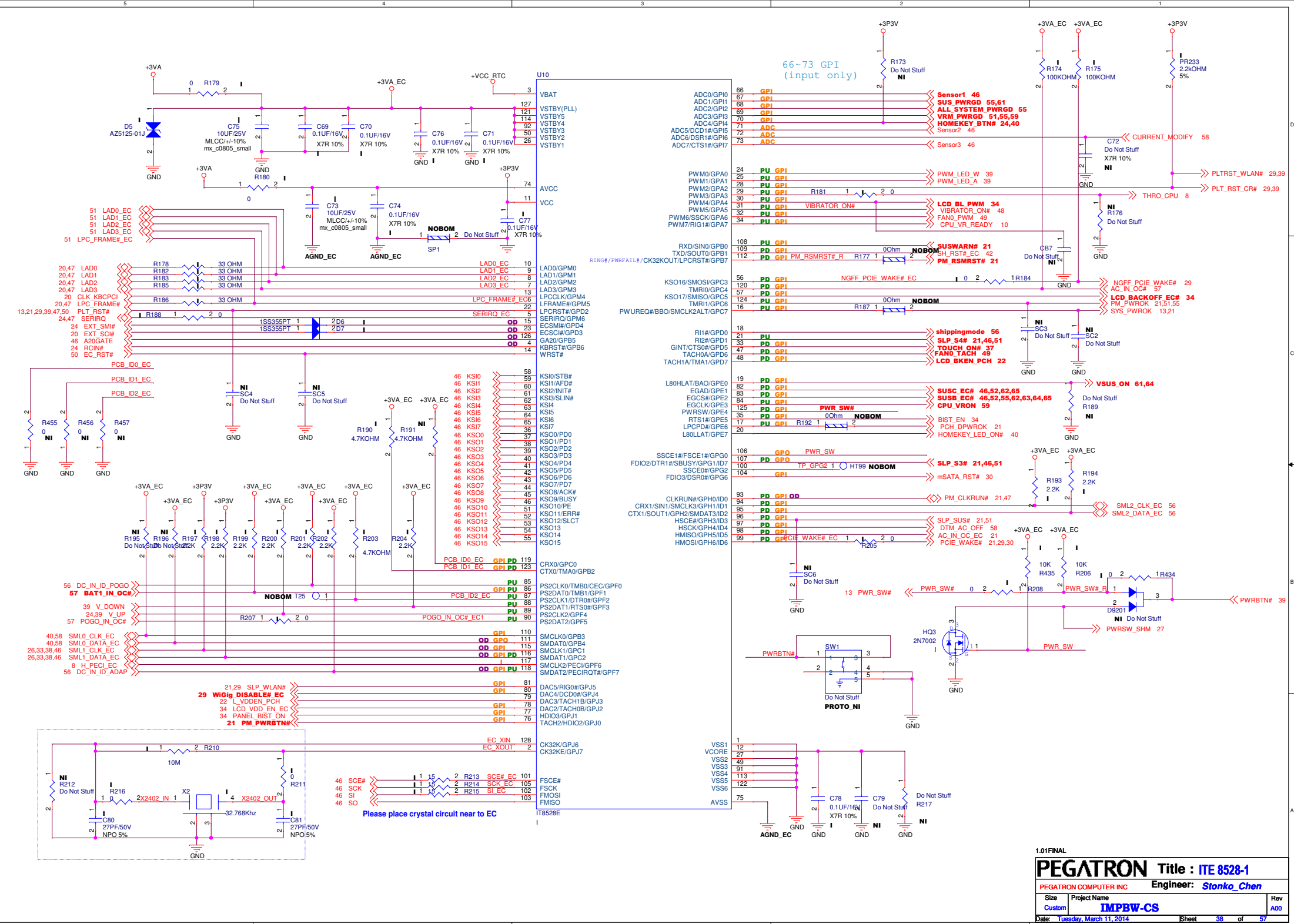


Gyro

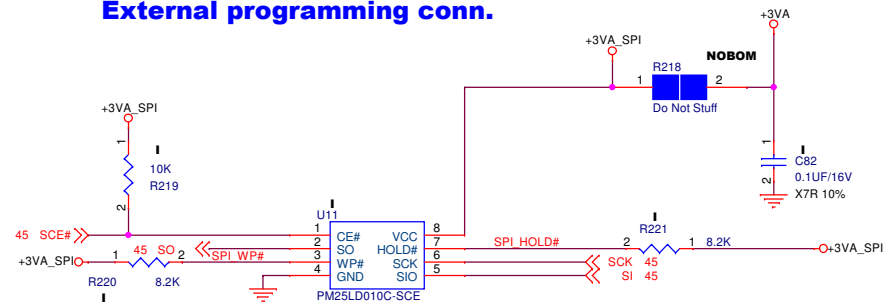


FFS





SPI ROM+ External programming conn.

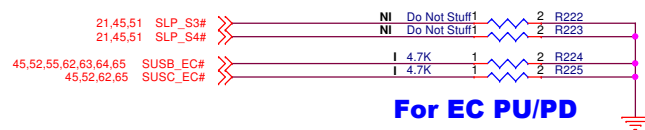


05X0022FC330 32Mb
0500-00P5000 (512Kb SPI)

Touch PAD(deleted)

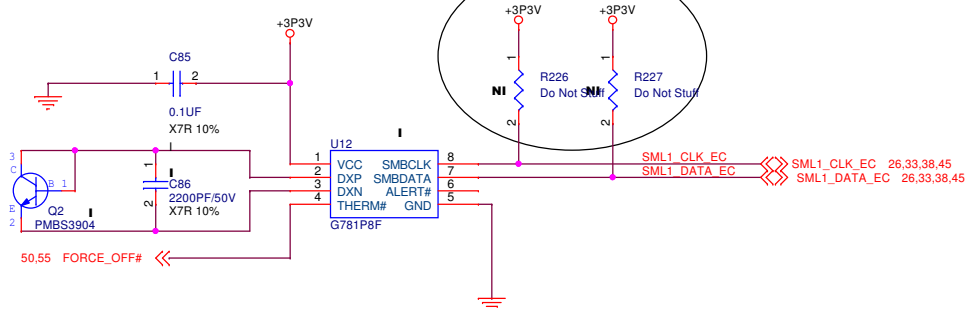
For Instant Key & Switch

Note: Close to EC

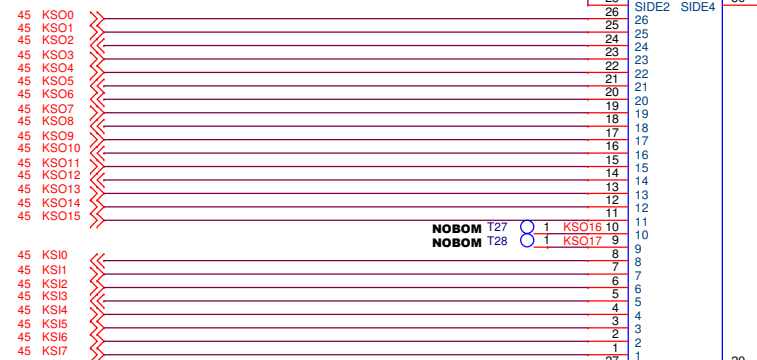


For EC PU/PD

place under DIMM

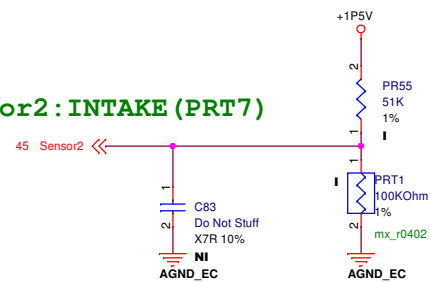


Keyboard Connector(debug)

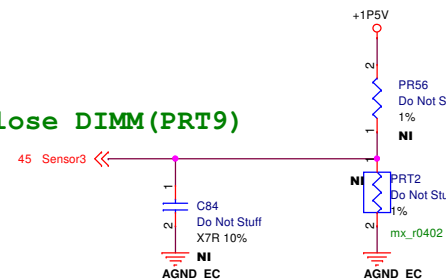


Debug Card CON

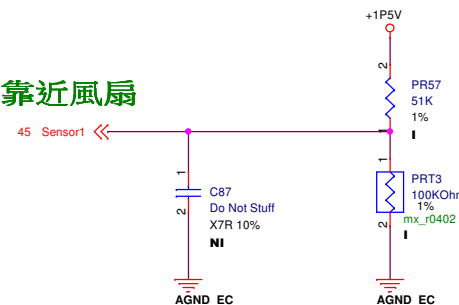
Sensor2 : INTAKE (PRT7)



close DIMM (PRT9)

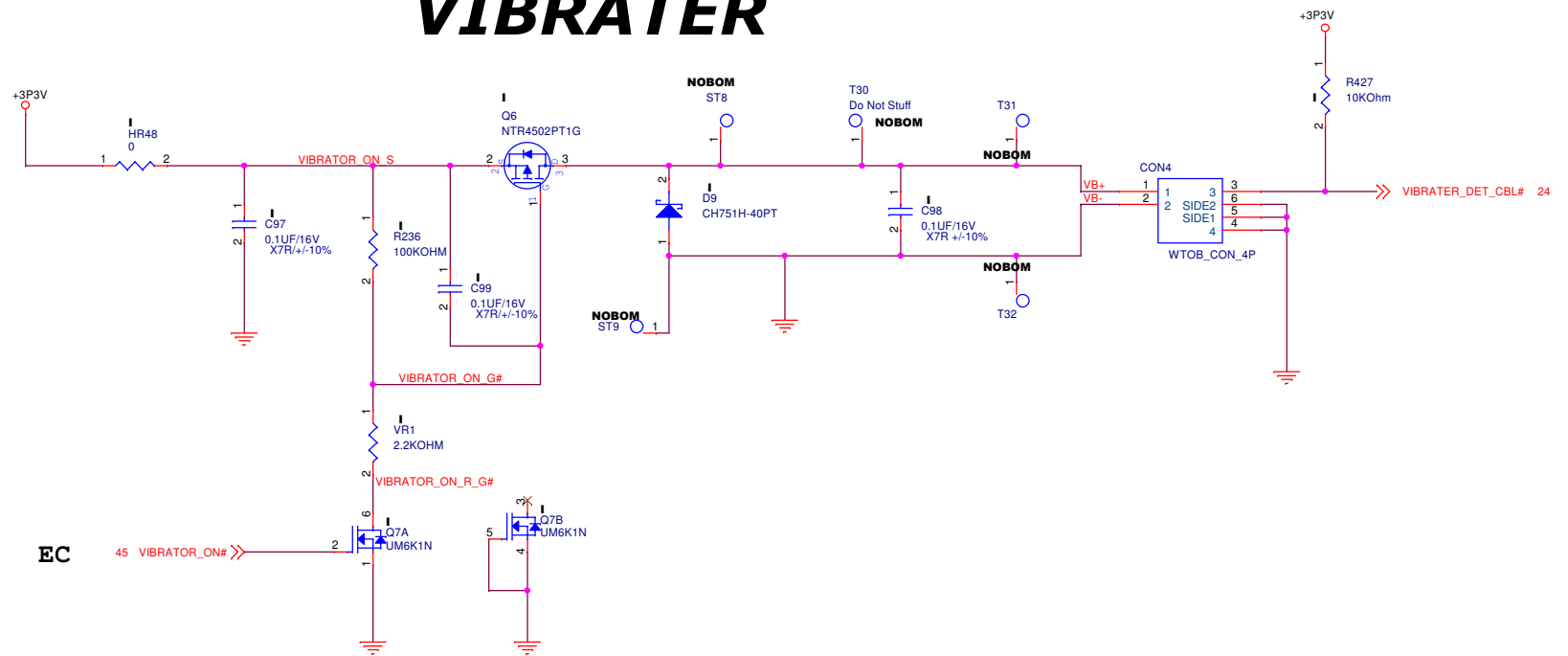


靠近風扇



1.01FINAL

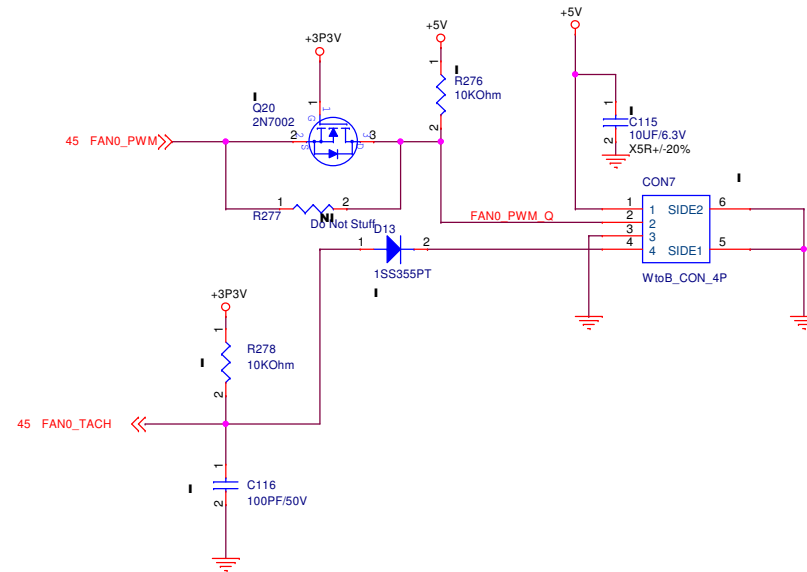
VIBRATER



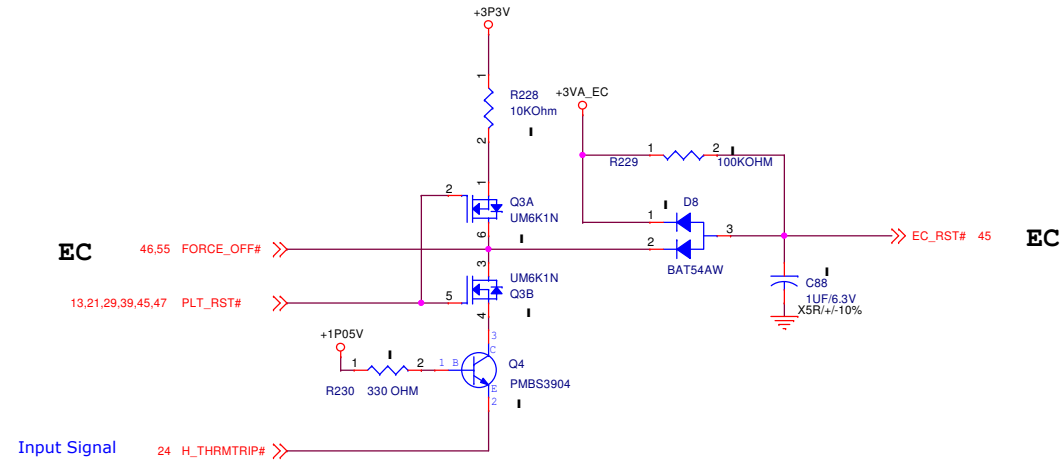
EC

```
45  VIBRATOR_ON# >>
```

PWM FAN



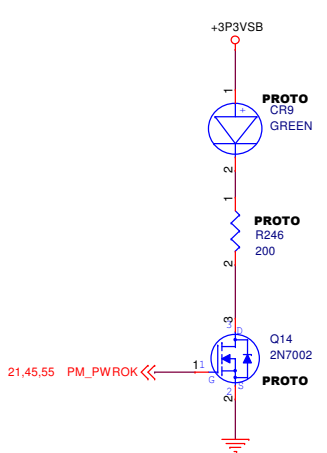
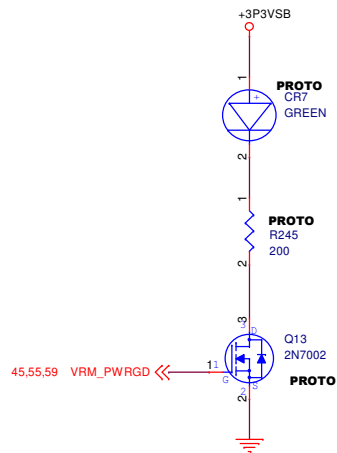
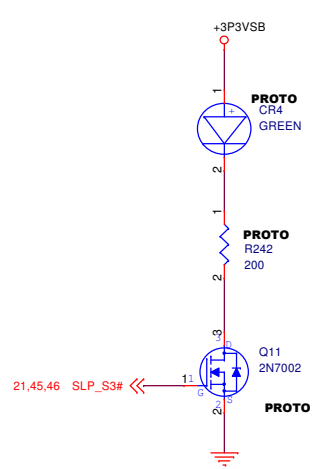
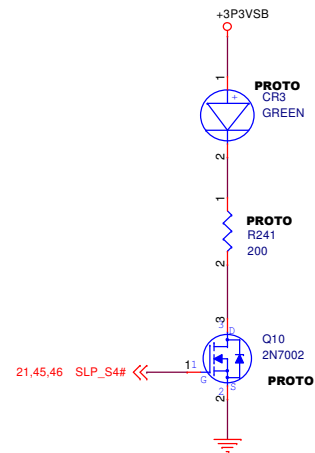
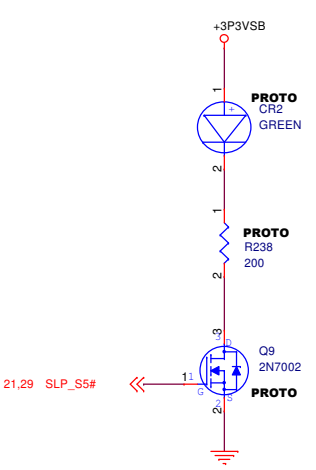
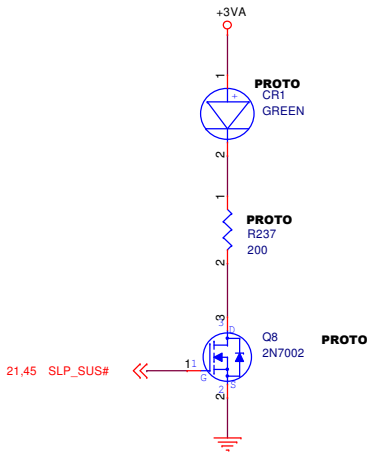
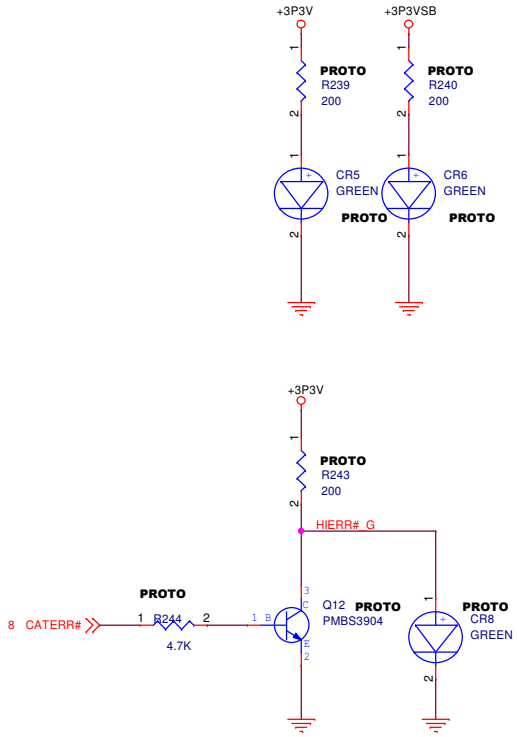
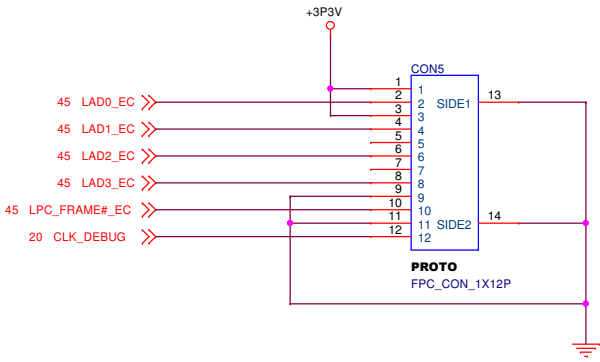
Thermal Policy



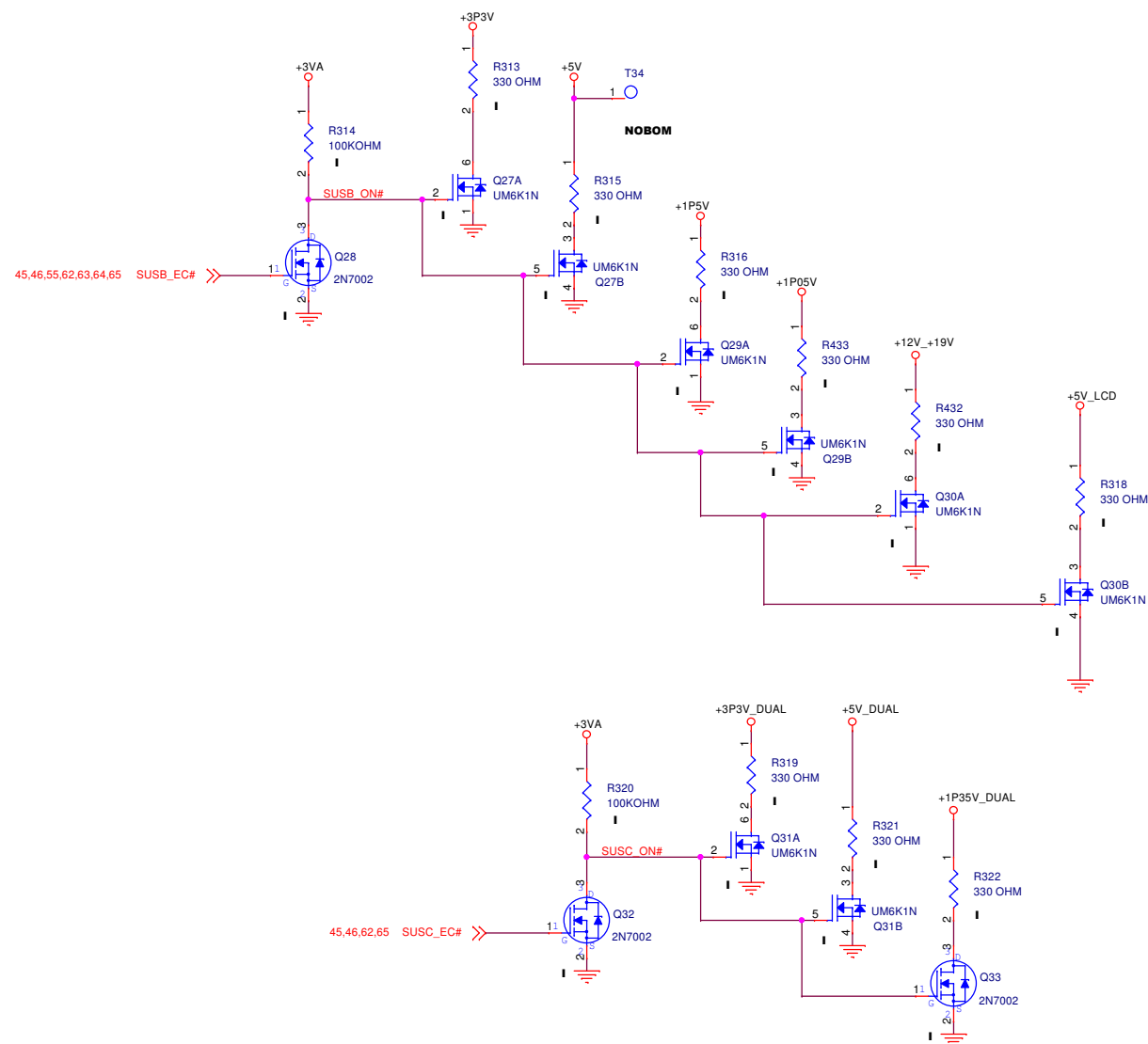
1.01FINAL

PEGATRON		Title : RST_Reset Circuit	
PEGATRON COMPUTER INC		Engineer: Stonko_Chen	
Size A3	Project Name IMPBW-CS	Rev A00	
Date: Tuesday, March 11, 2014		Sheet 43 of 57	

DEBUG CARD CONN.



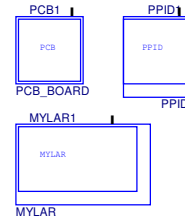
Discharge Circuit



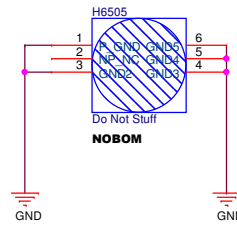
1.01FINAL

PEGATRON Title : **DSG_Discharge**
PEGATRON COMPUTER INC Engineer: **Stonko_Chen**

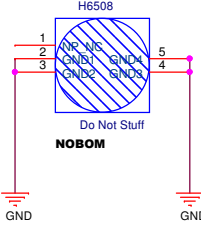
Size A3	Project Name IMPBW-CS	Rev A00
Date: Tuesday, March 11, 2014	Sheet 45 of 57	



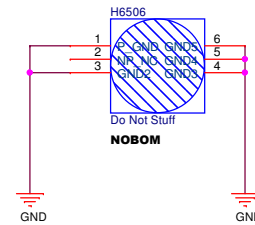
close fan



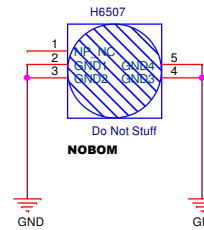
center



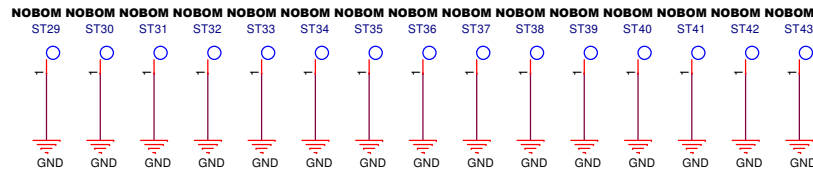
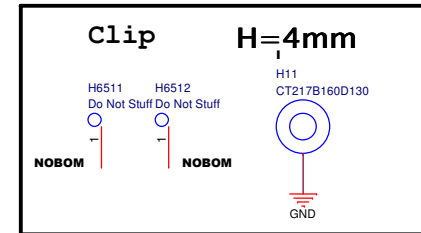
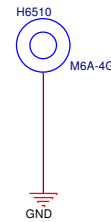
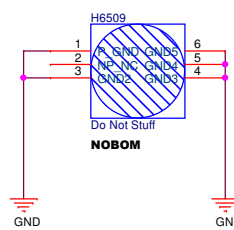
close CON5102



GND close L-IO



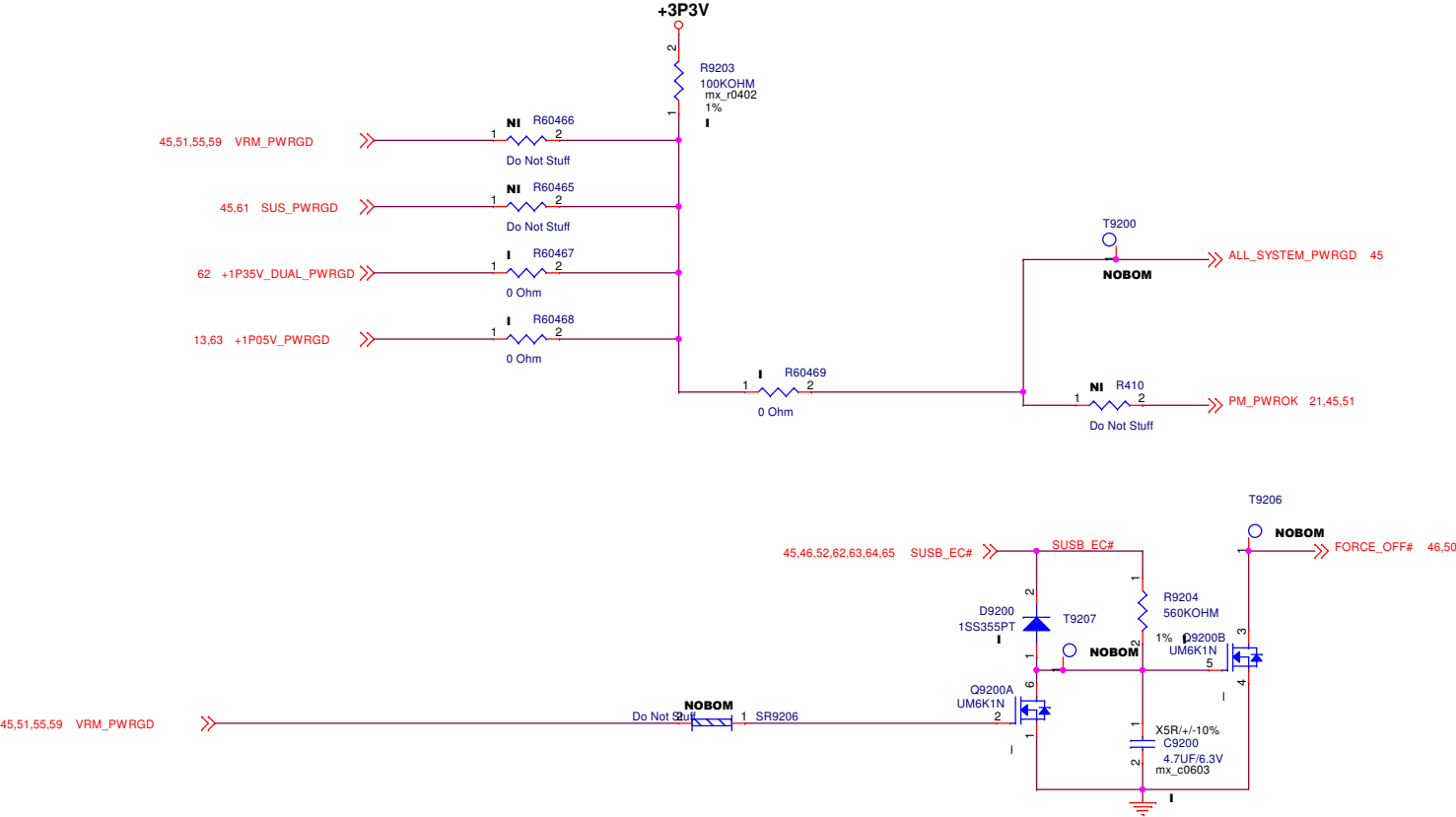
close R-IO



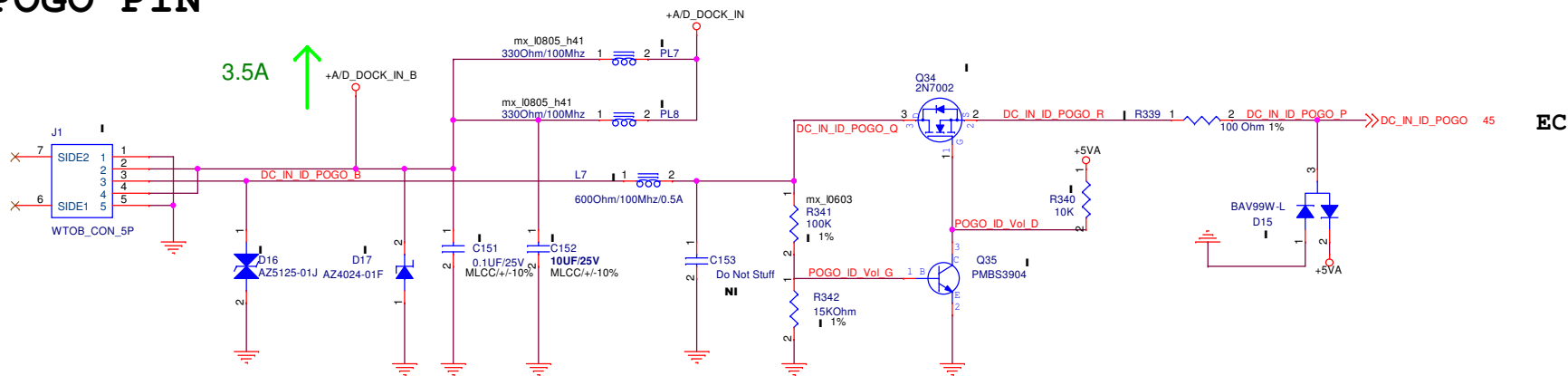
1.01FINAL

PEGATRON		Title :	screw
PEGATRON COMPUTER INC		Engineer:	Stonko_Chen
Size A3	Project Name IMPBW-CS	Rev A00	
Date: Tuesday, March 11, 2014		Sheet	46 of 57

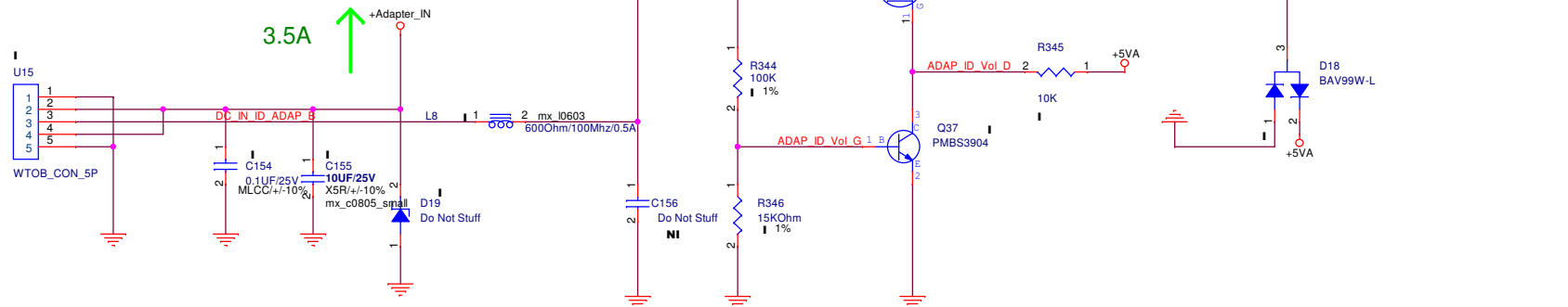
POWER GOOD DETECTOR



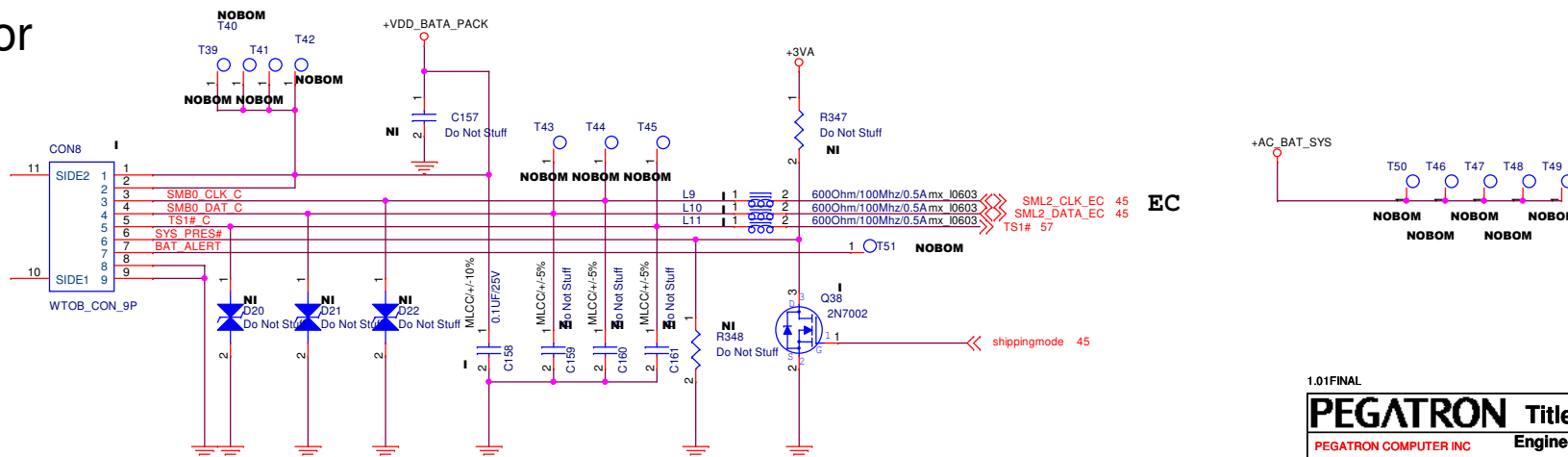
DC POGO PIN



DC JACK IN



Battery Connector



1.01FINAL

PEGATRON Title : **DC_DC/BAT CONN**

PEGATRON COMPUTER INC Engineer: **Stonko_Chen**

Size A3	Project Name IMPBW-CS	Rev A00
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Date: **Tuesday, March 11, 2014** Sheet **48** of **57**

POGO PIN

+A/D_DOCK_IN 3.5A →

3.5A ↑

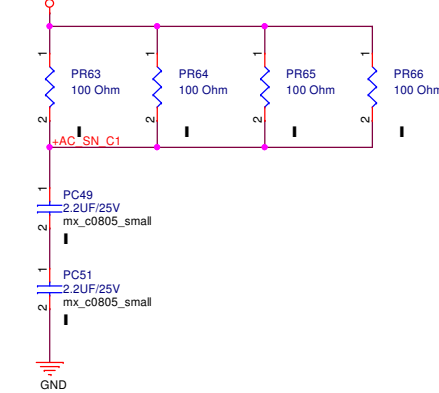
3.5A ←

DC Jack

DC IN

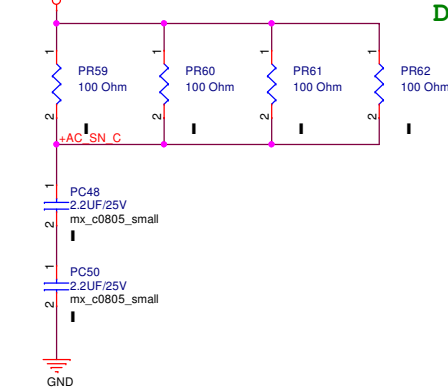
+Adapter_IN

+A/D_DOCK_IN

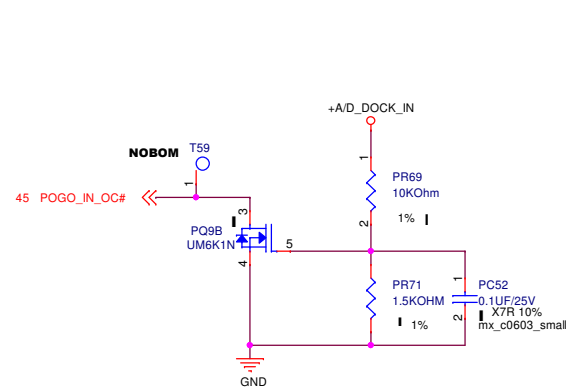


DOCKING IN DETECT

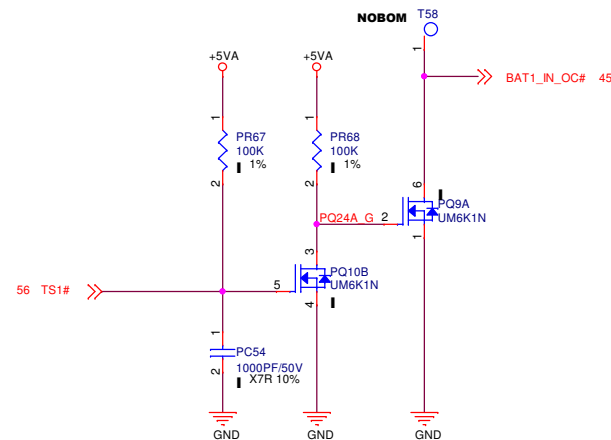
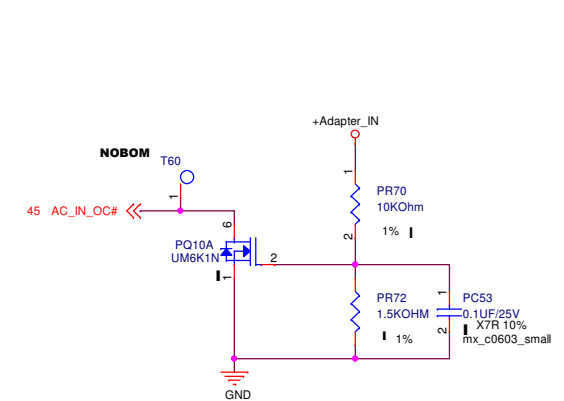
+Adapter_IN



Battery IN DETECT



ADAPTER IN DETECT



+Vcore
I_{max}=32A/TDC=10A for 15W
F_{sw}=1200KHz PL2=25W
PL2 TDC=14A
CSD97374CQ4M * 1



Processor TDP	Inductor size	Size Type	C, μ F	ESR, m Ω	ESL, nH	Supplier or PN
15W	0.47 μ H	0805 XSR	22 μ F 23x - Stuff 7x - no-stuff	3 m Ω	0.6 nH	TDK, Kyocera, Murata, Taiyo-Yudaein, Samsung
28W			22 μ F 26x - Stuff 4x - no-stuff			

Note: See the manufacturer data sheet for more details.

1.01FINAL

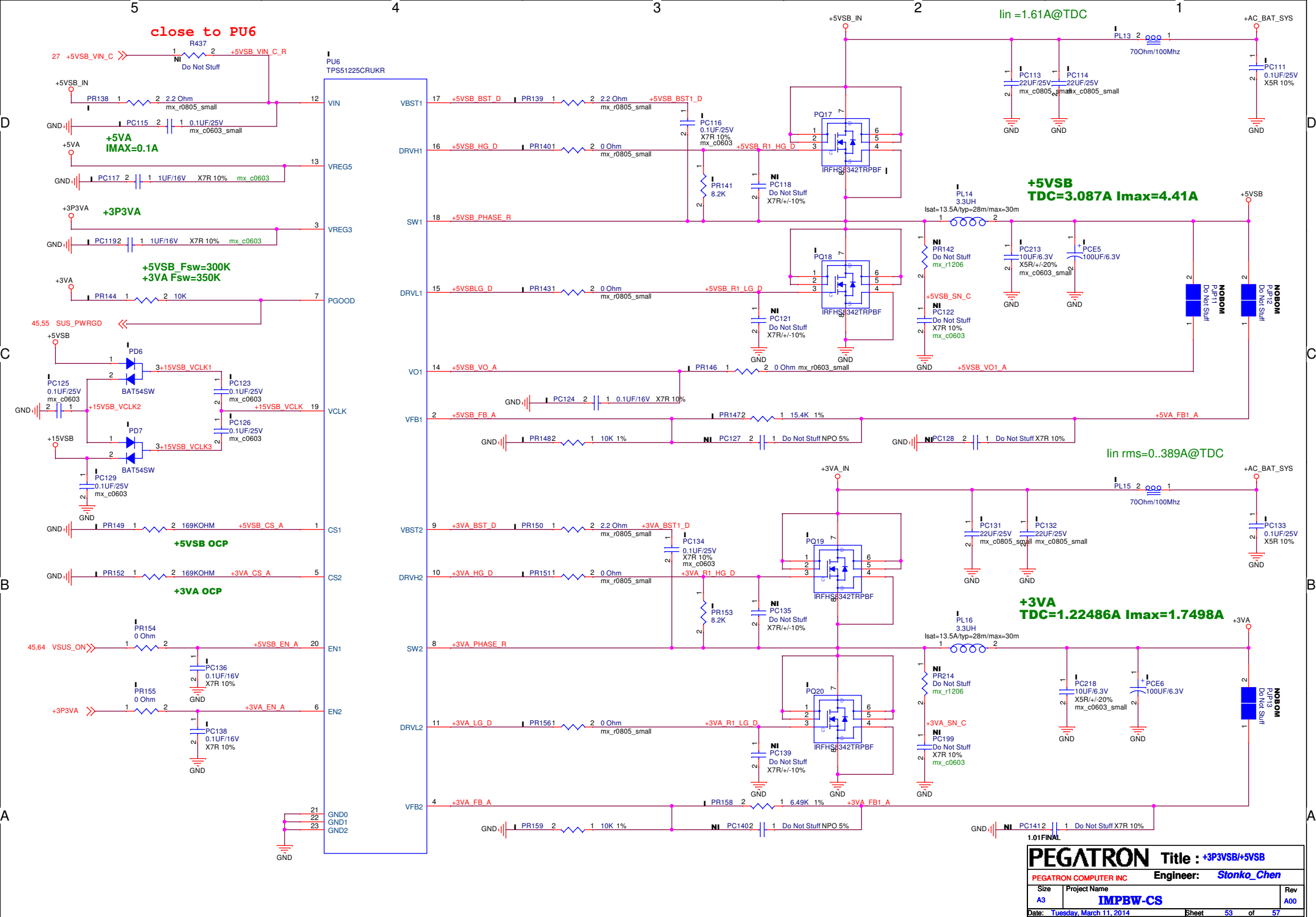
PEGATRON Title : +VCORE1

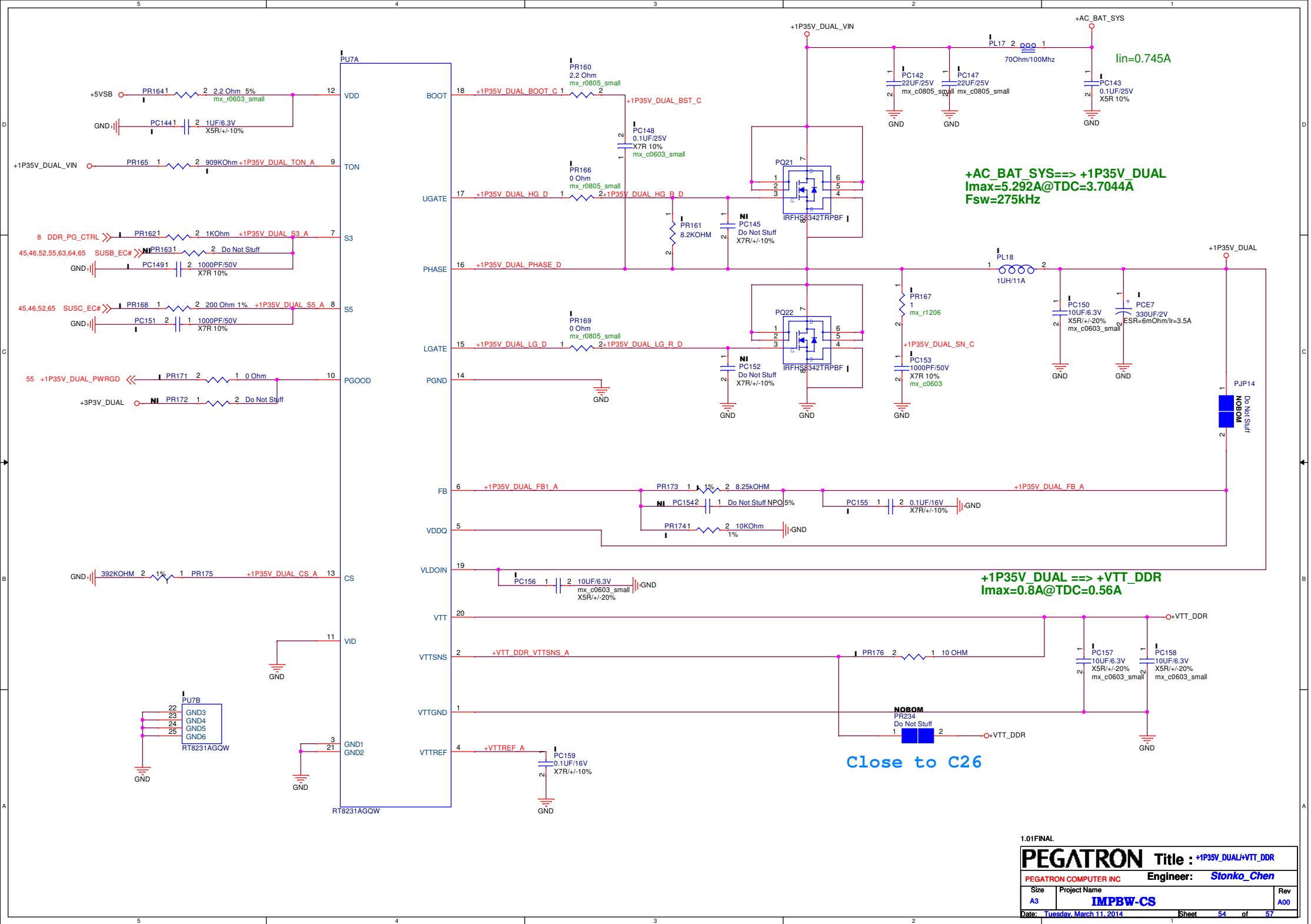
PEGATRON COMPUTER INC Engineer: *Stonko_Chen*

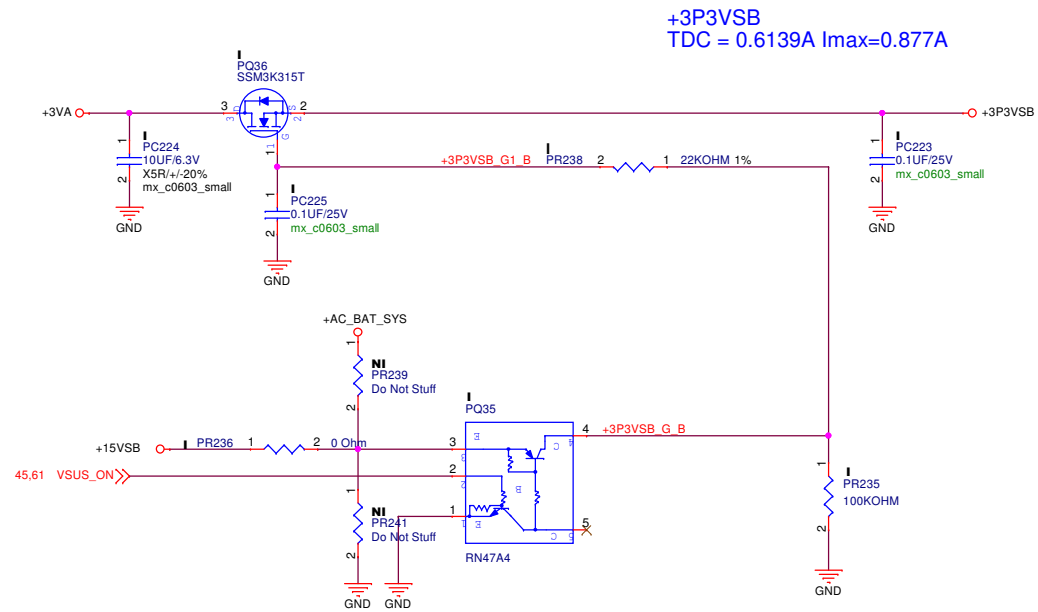
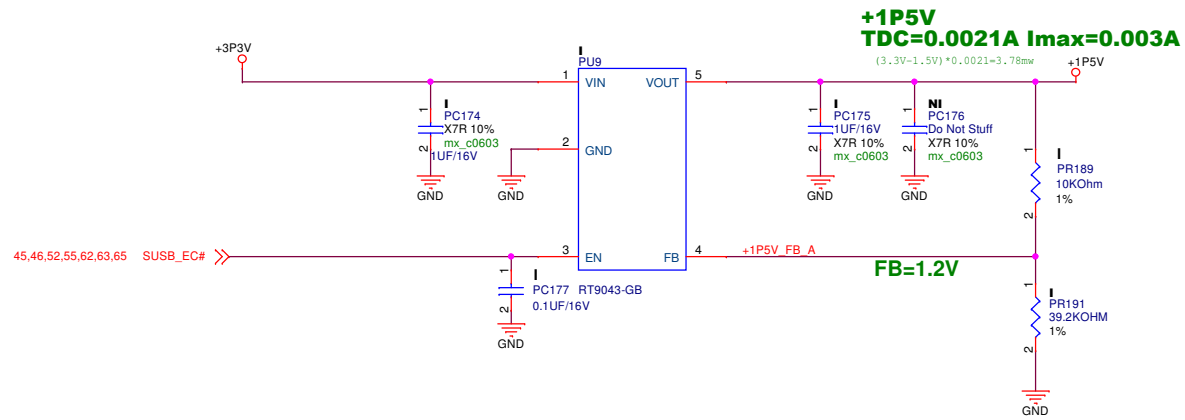
Size	Project Name	Rev
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Date: Tuesday, March 11, 2014 Sheet 52 of 57

Date: Tuesday, March 11, 2014 Sheet 32 of 37







1.01FINAL

PEGATRON		Title : +1P5V +3P3VSB	
PEGATRON COMPUTER INC		Engineer: <u>Stonko_Chen</u>	
Size A3	Project Name IMPBW-CS		Rev A00
Date: Tuesday, March 11, 2014		Sheet 56 of 57	

